

BEST AVAILABLE COPY

1150

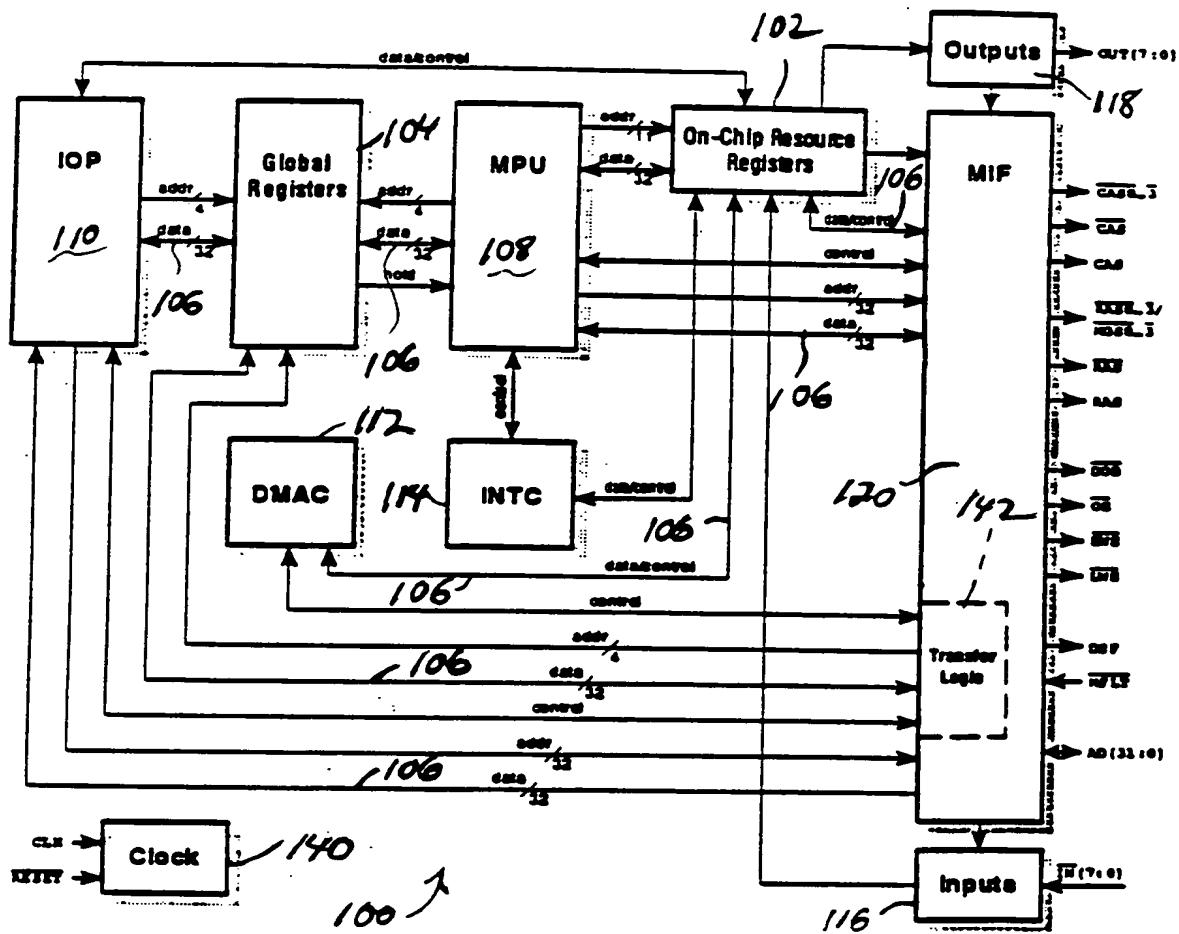


FIG. 1

2/50

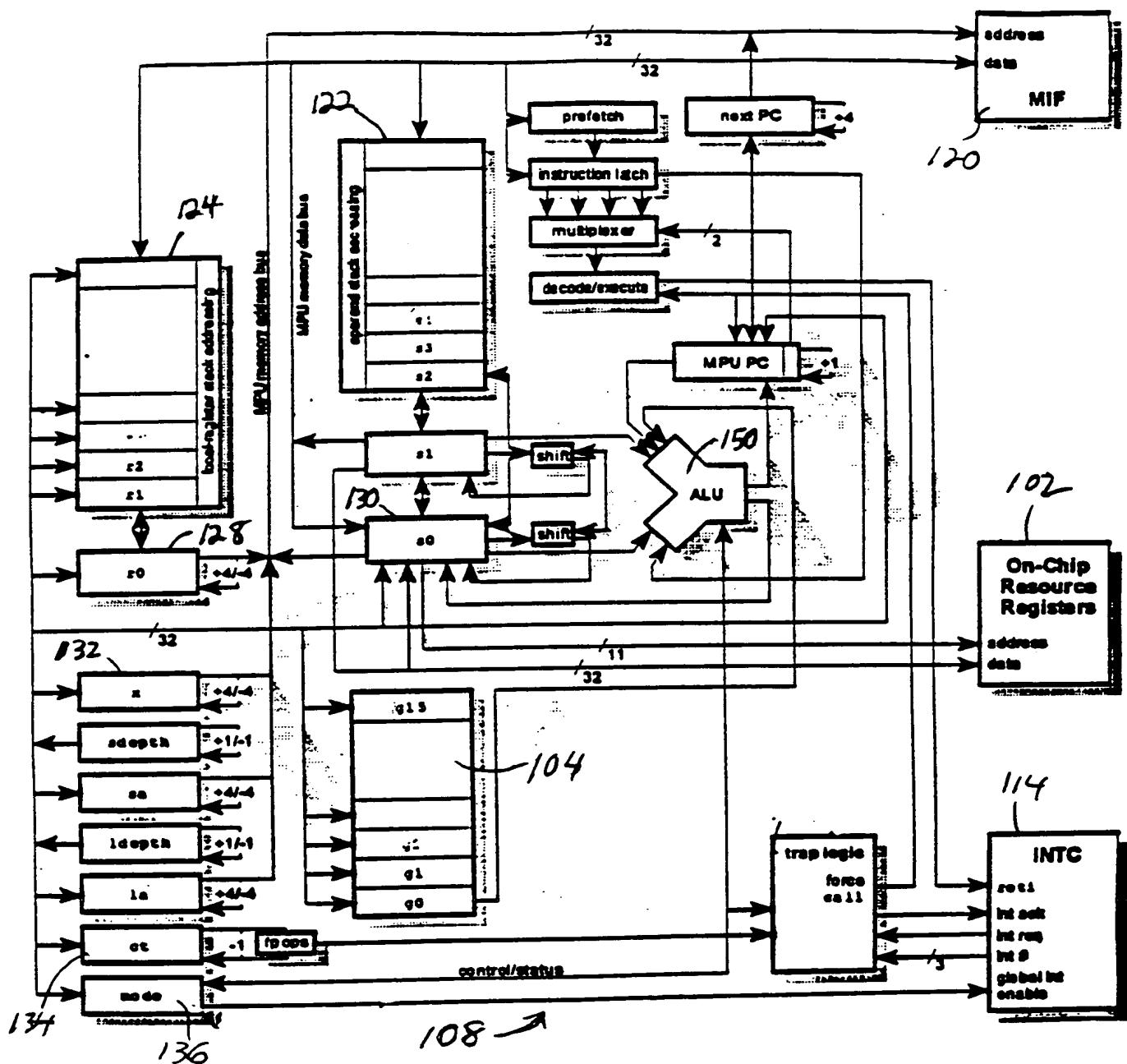


FIG. 2

3/50

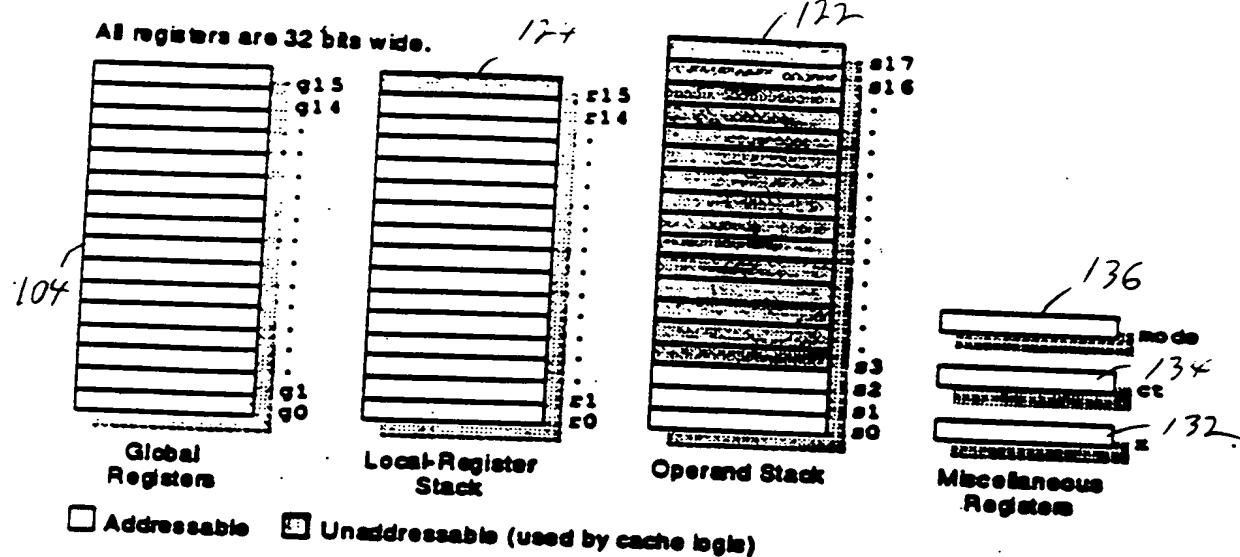


FIG. 3

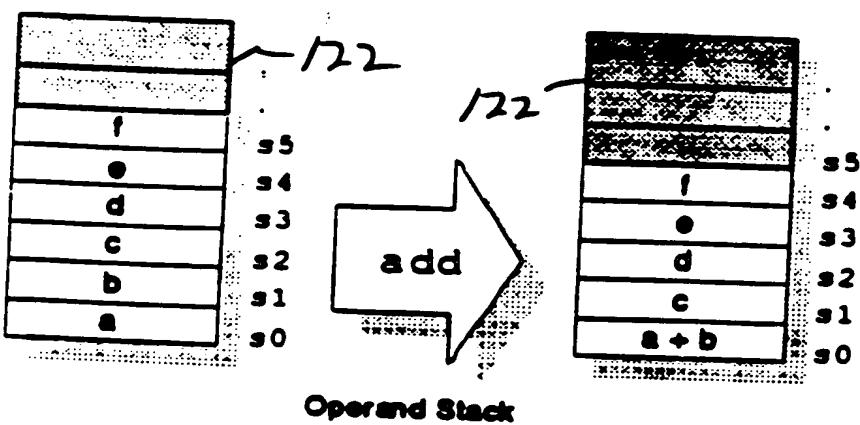


FIG. 3a

4/50

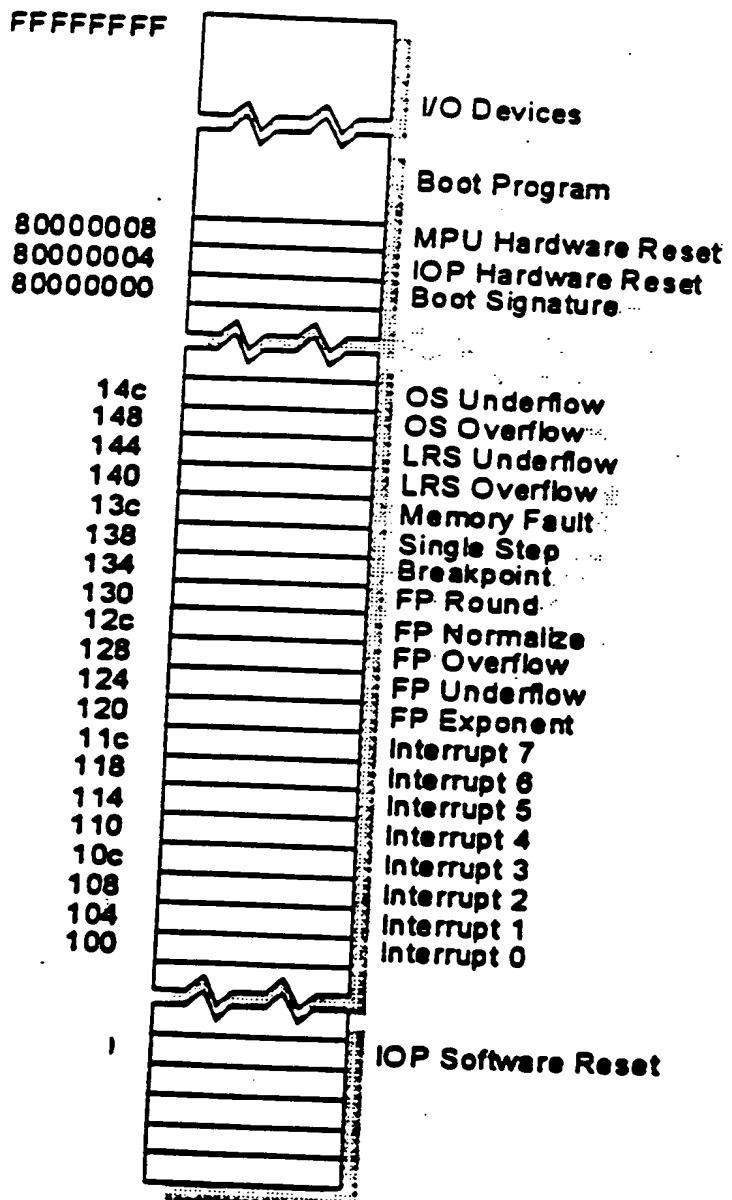


Fig. 4

5/50

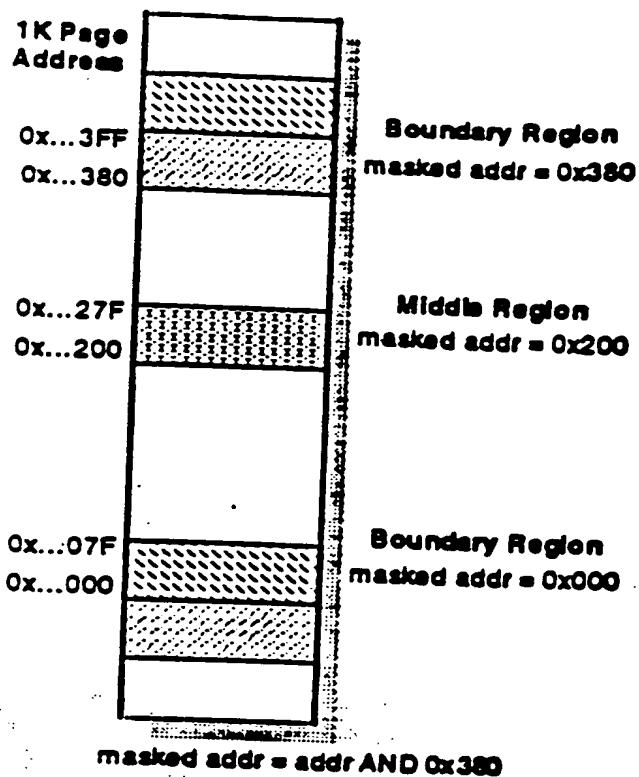


Fig. 5

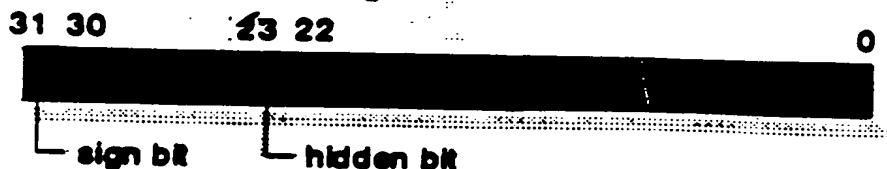
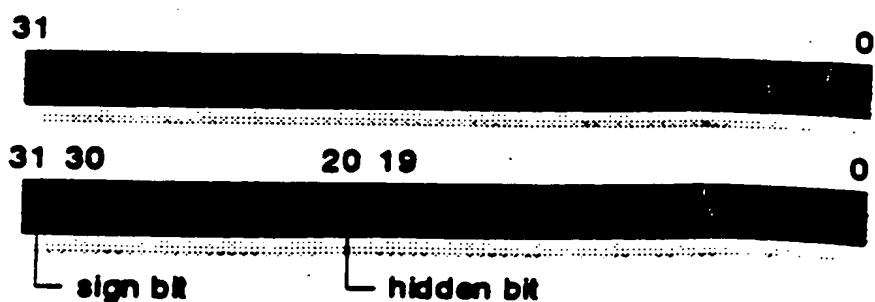
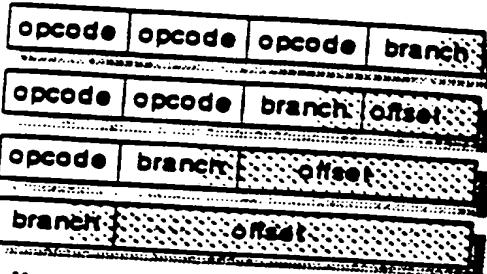
Single Precision**Double Precision**

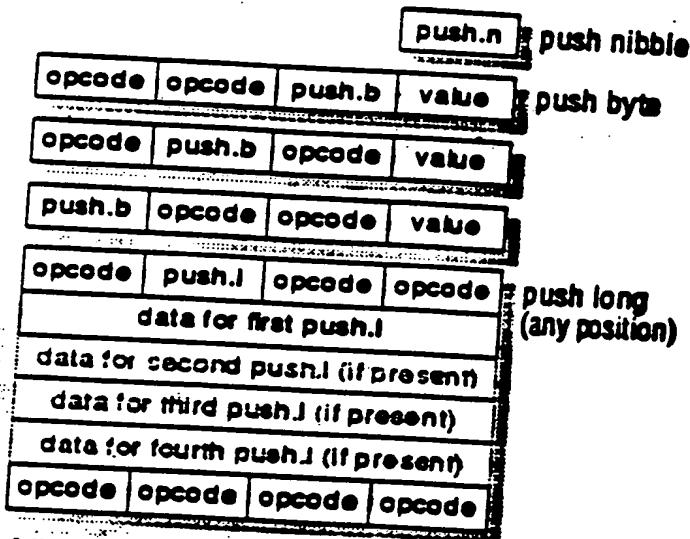
Fig. 6a

6/50

Branches



Literals



All Others



FIG. 6

7/50

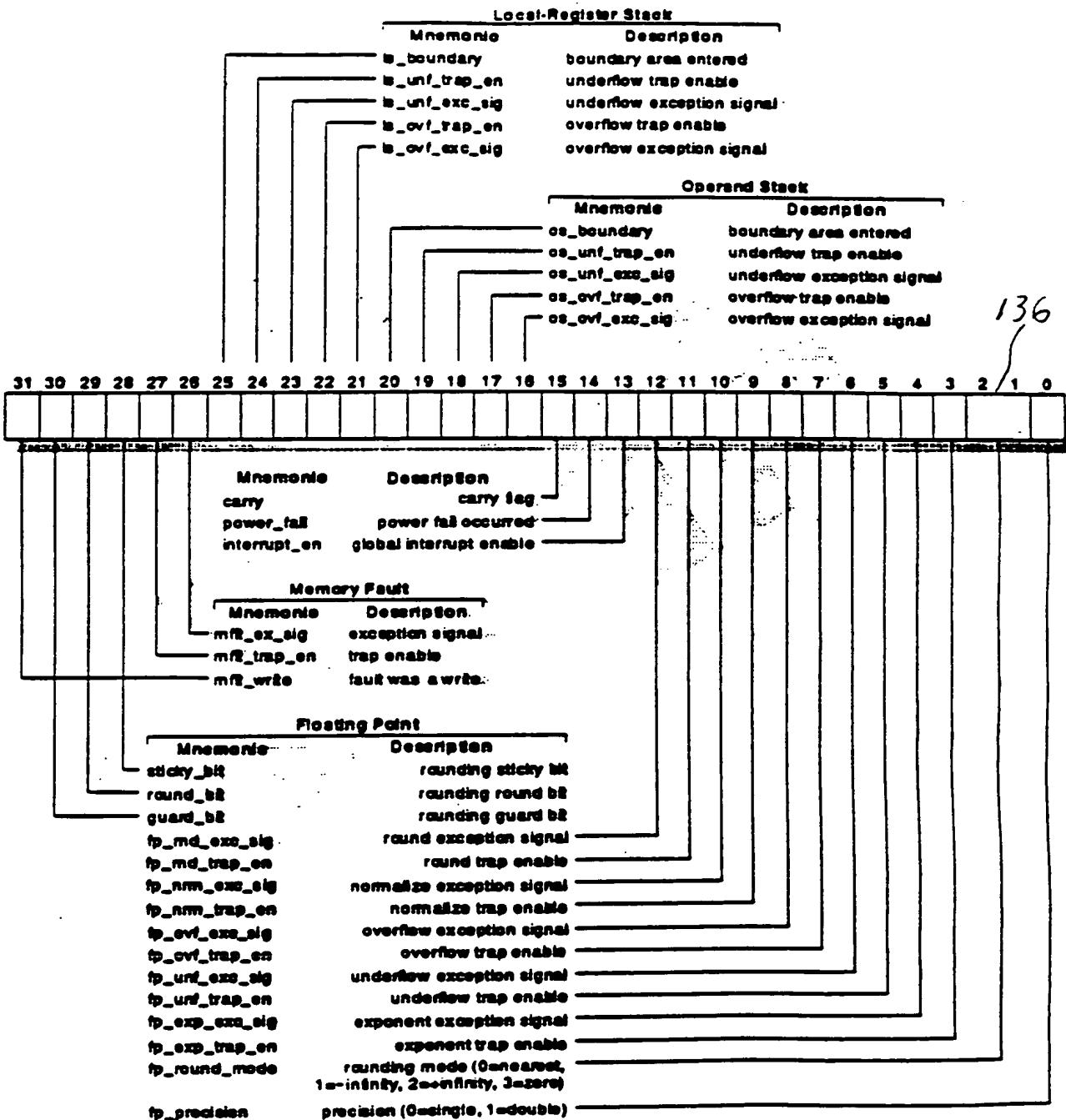


Fig. 7

8/50

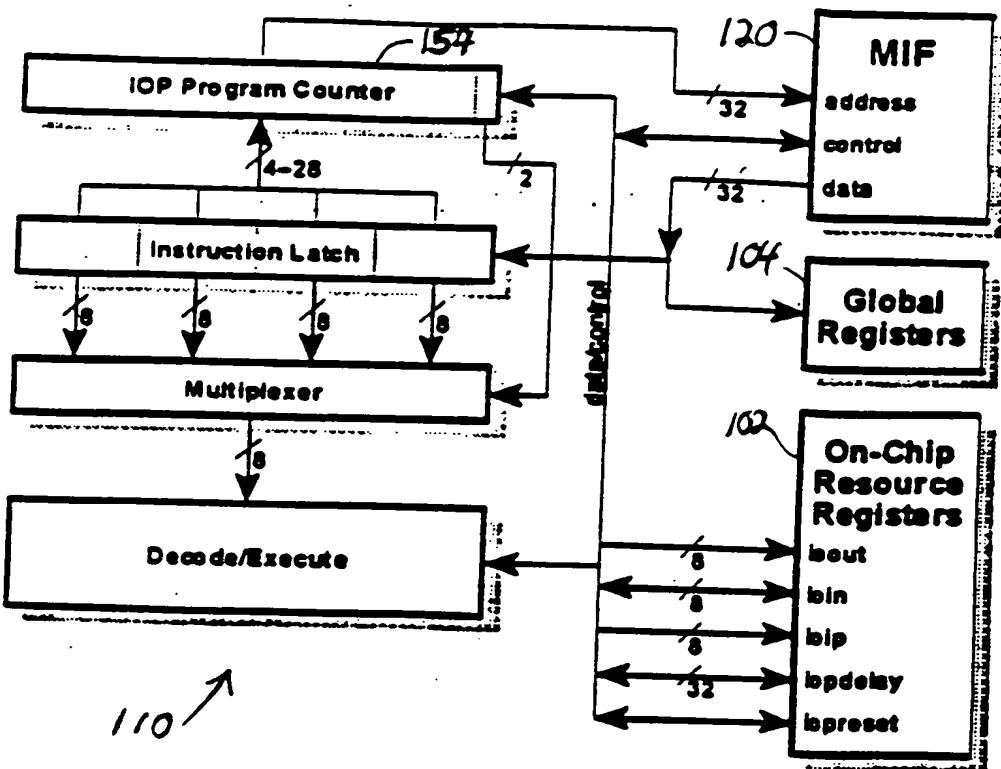


FIG. 8

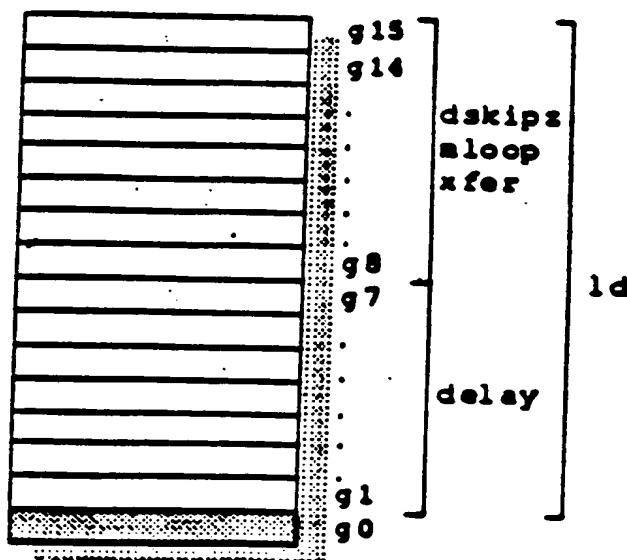
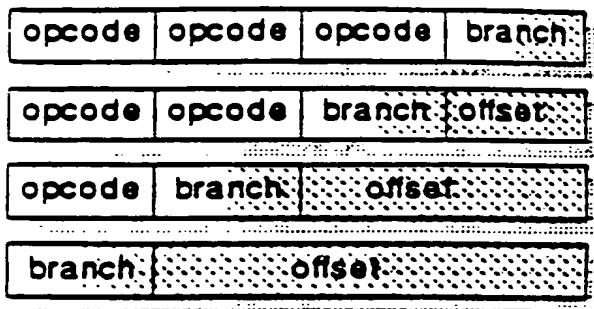


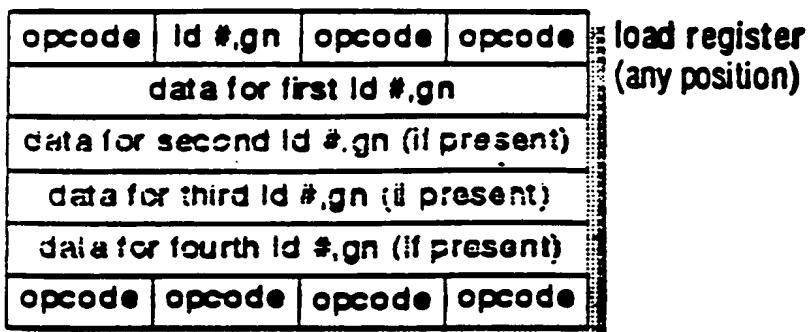
FIG. 9

9/50

Branches



Literals



All Others

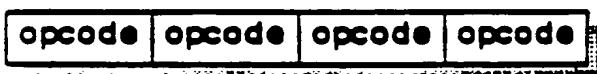


FIG. 10

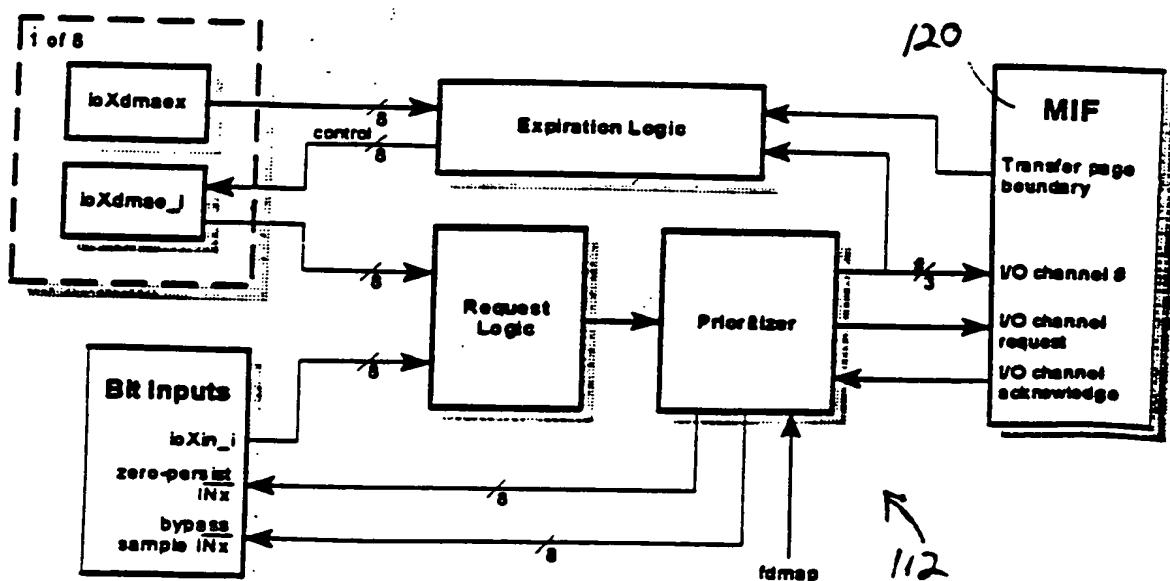


FIG. 11

10/50

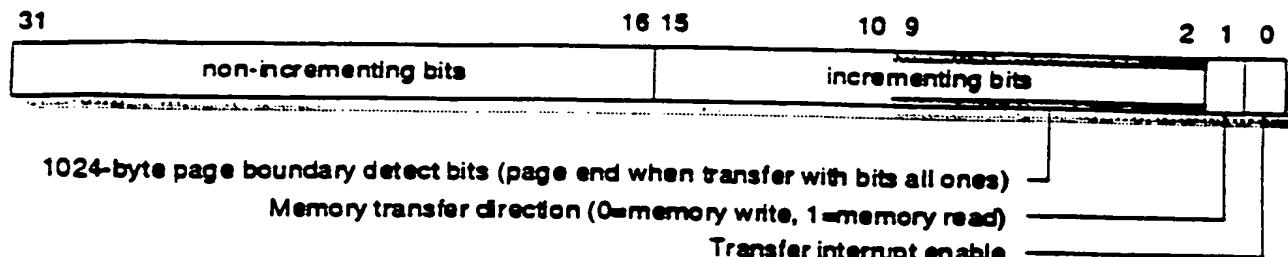


Fig. 12

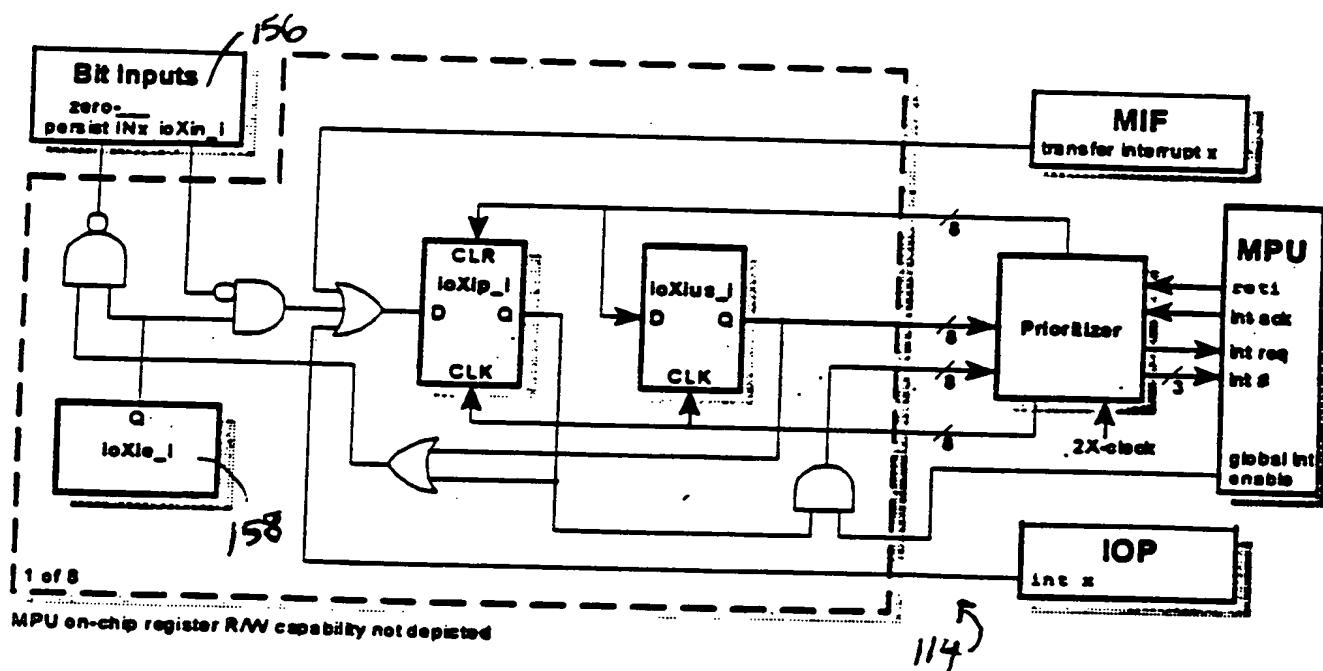


FIG. 13

111/52

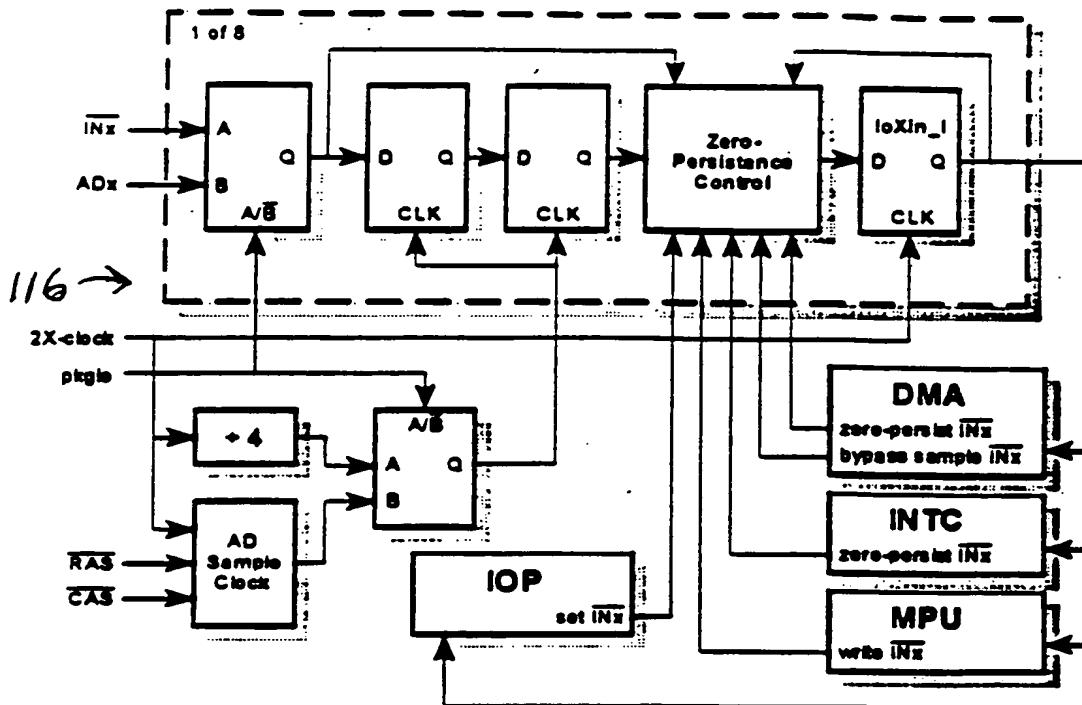


FIG. 14

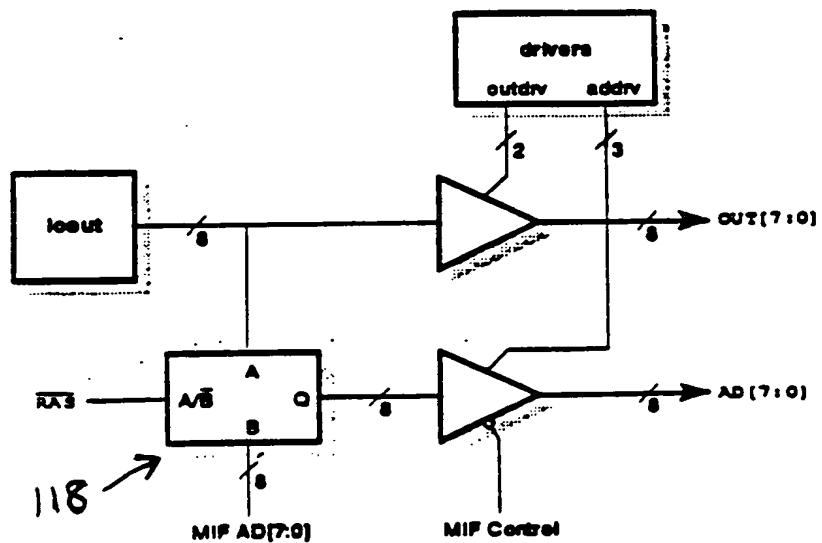


FIG. 15

12/52

SMB — Single Memory Bank per Memory Group Mode

31

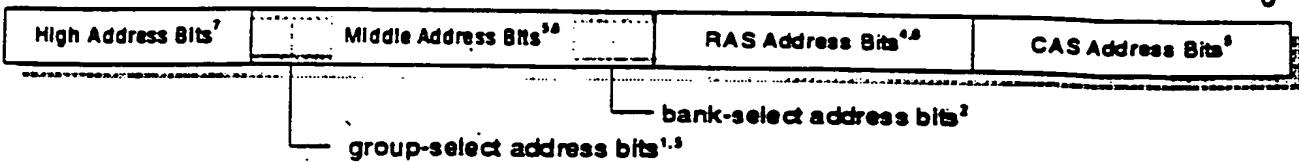
0



MMB — Multiple Memory Bank per Memory Group Mode

31

0



Notes

1. Located by bits in msg sm.
2. DRAM—2 bits immediately above the RAS address bits.
SRAM—2 bits located by msg sm in misc.
3. SRAM and DRAM.
4. DRAM only, field is zero length in SRAM.
5. Excluded from RAS-cycle determination, except for A31 (see note 7).
6. Included in RAS-cycle determination.
7. Optionally included in RAS-cycle determination.
8. If msg sm is zero, see text.

FIG. 16

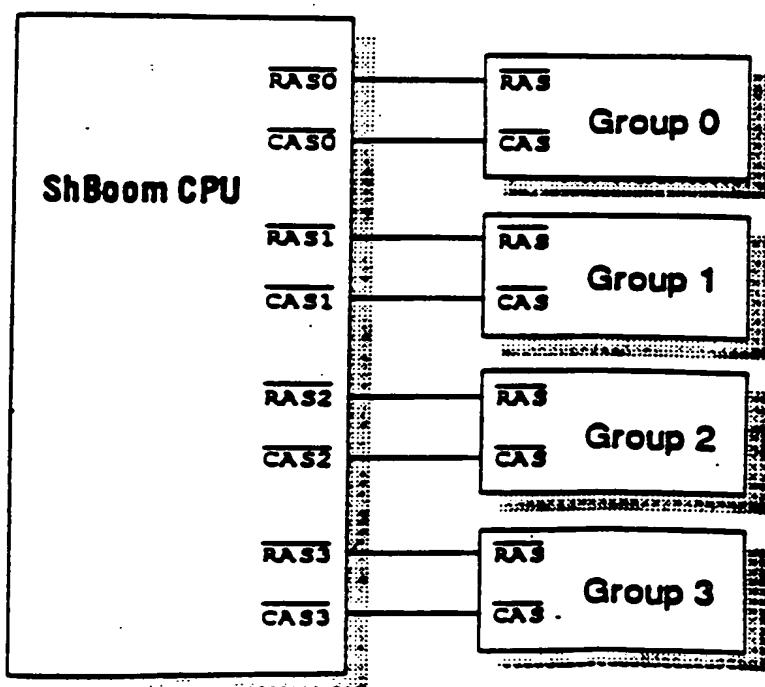


FIG. 17

13/50

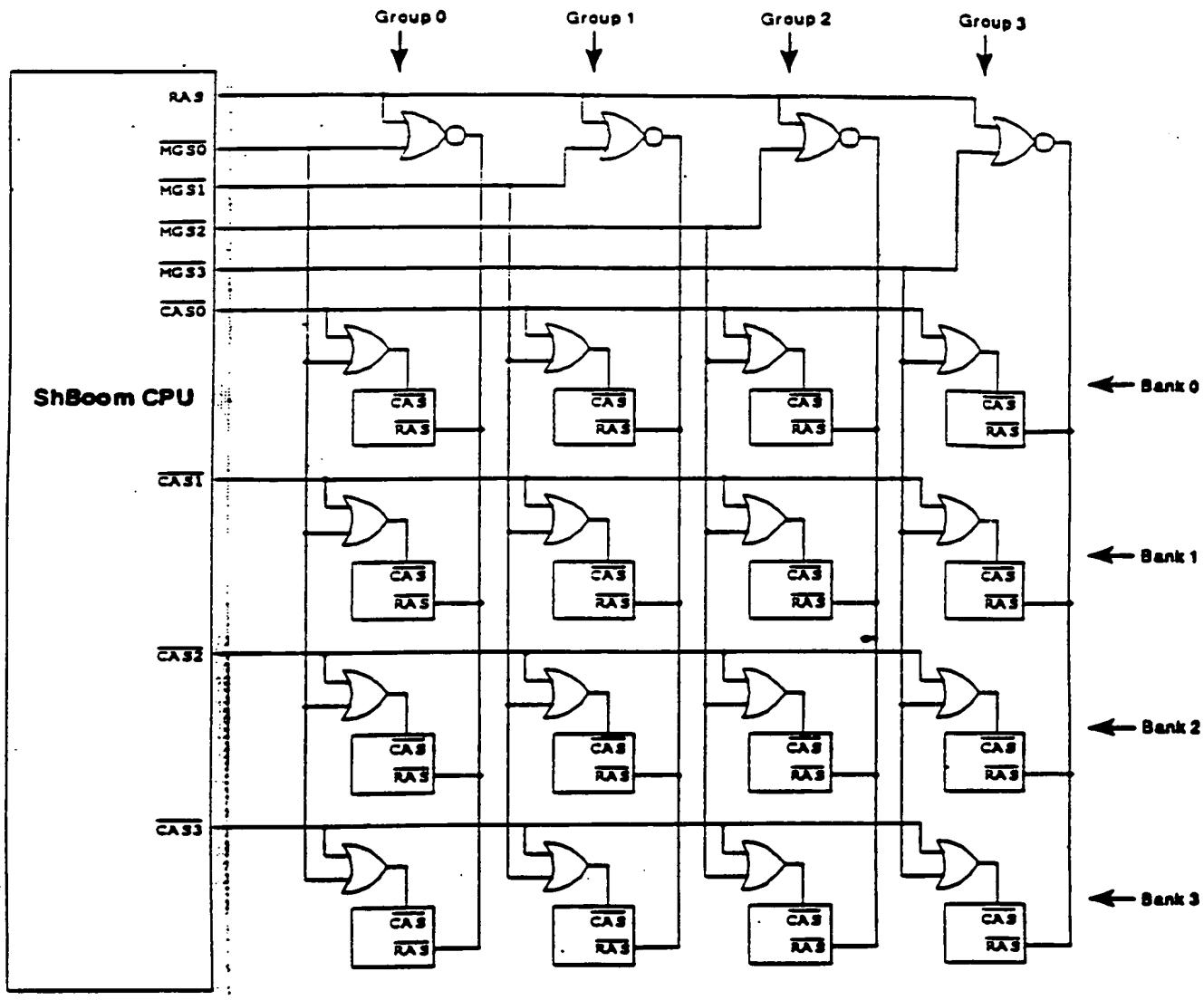


FIG. 18

14/50

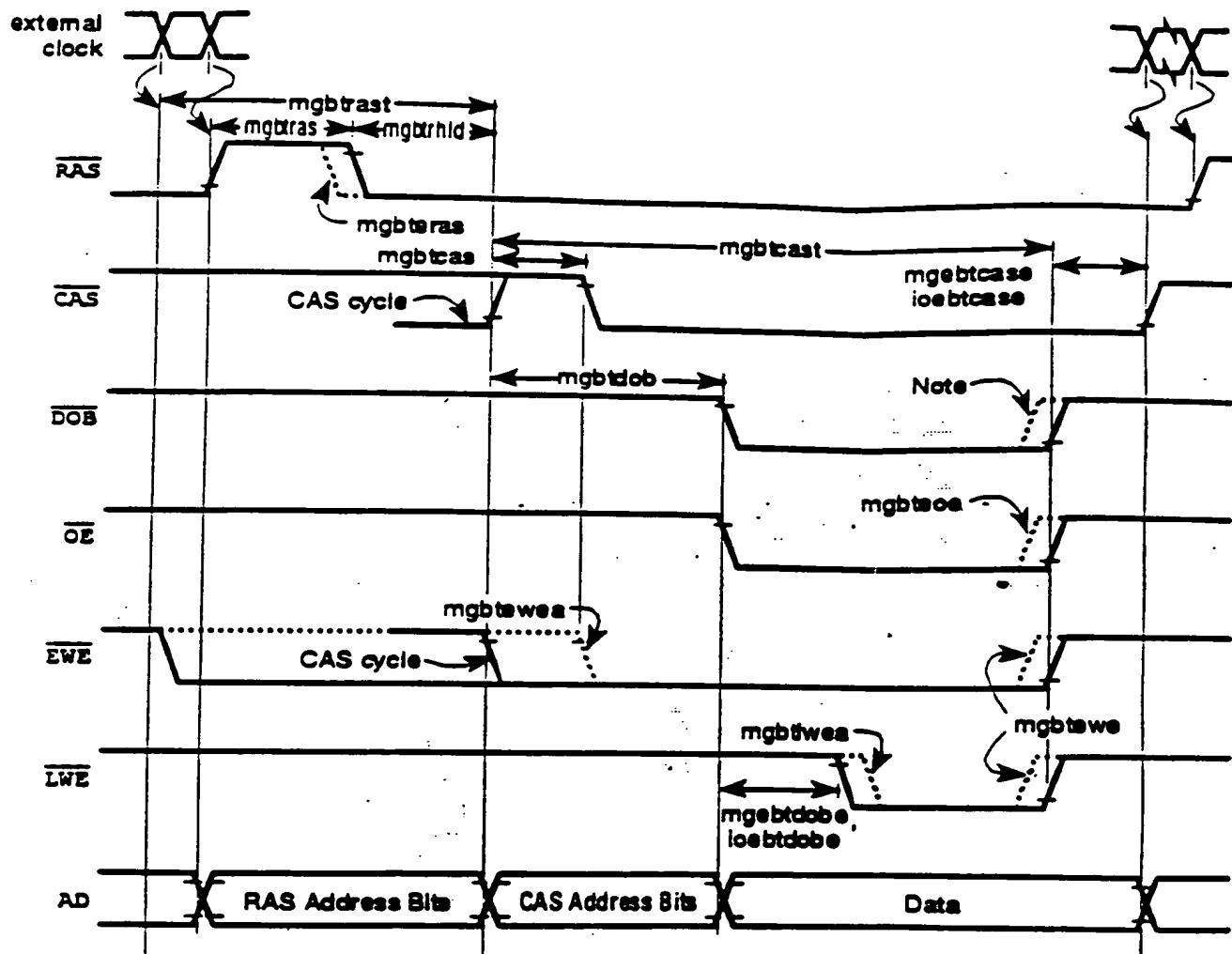


FIG. 19

09/051263

WO 97/15001

PCT/US96/16013

15/50

Register Size	Addr	Mnemonic	Description
31	15 13 10 7 0		
		ioin	Bit Input Register
		ioip	Interrupt Pending Register
		iosr	Interrupt Under Service Register
		ioct	Bit Output Register
		ioen	Interrupt Enable Register
		iodmae	DMA Enable Register
		vram	VRAM Control Bit Register
		miaca	Miscellaneous A Register
		miabc	Miscellaneous B Register
		mfaddr	Memory Fault Address Register
		mfdata	Memory Fault Data Register
		msm	Memory System Group Select Mask Register
		mgds	Memory Group Device Size Register
		miacc	Miscellaneous C Register
		mg0ext	Memory Group 0 Extended Bus Timing Register
		mg1ext	Memory Group 1 Extended Bus Timing Register
		mg2ext	Memory Group 2 Extended Bus Timing Register
		mg3ext	Memory Group 3 Extended Bus Timing Register
		mg0cas	Memory Group 0 CAS Bus Timing Register
		mg1cas	Memory Group 1 CAS Bus Timing Register
		mg2cas	Memory Group 2 CAS Bus Timing Register
		mg3cas	Memory Group 3 CAS Bus Timing Register
		mg0ras	Memory Group 0 RAS Bus Timing Register
		mg1ras	Memory Group 1 RAS Bus Timing Register
		mg2ras	Memory Group 2 RAS Bus Timing Register
		mg3ras	Memory Group 3 RAS Bus Timing Register
		io0ext	VO Channel 0 Extended Bus Timing Register
		io1ext	VO Channel 1 Extended Bus Timing Register
		io2ext	VO Channel 2 Extended Bus Timing Register
		io3ext	VO Channel 3 Extended Bus Timing Register
		io4ext	VO Channel 4 Extended Bus Timing Register
		io5ext	VO Channel 5 Extended Bus Timing Register
		io6ext	VO Channel 6 Extended Bus Timing Register
		io7ext	VO Channel 7 Extended Bus Timing Register
		msra	Memory System Refresh Address Register (WO)
		ioptdy	IOP Delay Register (IO)
		iodtta	VO Device Transfer Types A Register
		iodtta	VO Device Transfer Types B Register
		iodmaez	VO DMA Enable Expiration Register
		dcrcr	Driver Current Register
		ioreset	IOP Reset Register

Fig. 20

Bit Input Register		8 7 6 5 4 3 2 1 0
31		
Reserved Zeros		
Bit Address	Mnemonic	Description
07	io7in_J	I/O bit 7 Input
06	io6in_J	I/O bit 6 Input
05	io5in_J	I/O bit 5 Input
04	io4in_J	I/O bit 4 Input
03	io3in_J	I/O bit 3 Input
02	io2in_J	I/O bit 2 Input
01	io1in_J	I/O bit 1 Input
00	io0in_J	I/O bit 0 Input

Fig. 21

16/50

20 ioip **Interrupt Pending Register**

31

8 7 6 5 4 3 2 1 0

Reserved Zeros

BR Address	Mnemonic	Description
27	io7ip_J	I/O bit 7 interrupt pending
26	io6ip_J	I/O bit 6 interrupt pending
25	io5ip_J	I/O bit 5 interrupt pending
24	io4ip_J	I/O bit 4 interrupt pending
23	io3ip_J	I/O bit 3 interrupt pending
22	io2ip_J	I/O bit 2 interrupt pending
21	io1ip_J	I/O bit 1 interrupt pending
20	io0ip_J	I/O bit 0 interrupt pending

FIG. 22

40 ious **Interrupt Under Service Register**

31

8 7 6 5 4 3 2 1 0

Reserved Zeros

BR Address	Mnemonic	Description
47	io7ius_J	I/O bit 7 interrupt under service
46	io6ius_J	I/O bit 6 interrupt under service
45	io5ius_J	I/O bit 5 interrupt under service
44	io4ius_J	I/O bit 4 interrupt under service
43	io3ius_J	I/O bit 3 interrupt under service
42	io2ius_J	I/O bit 2 interrupt under service
41	io1ius_J	I/O bit 1 interrupt under service
40	io0ius_J	I/O bit 0 interrupt under service

FIG 23

60 iocut **Bit Output Register**

31

8 7 6 5 4 3 2 1 0

Reserved Zeros

BR Address	Mnemonic	Description
67	io7out_J	I/O bit 7 output
66	io6out_J	I/O bit 6 output
65	io5out_J	I/O bit 5 output
64	io4out_J	I/O bit 4 output
63	io3out_J	I/O bit 3 output
62	io2out_J	I/O bit 2 output
61	io1out_J	I/O bit 1 output
60	io0out_J	I/O bit 0 output

FIG. 24

17/50

801ole Interrupt Enable Register

31

8 7 6 5 4 3 2 1 0

Reserved Zeros											
Bit Address	Mnemonic	Description									
87	io7ie_j	I/O bit 7 interrupt enable									
86	io6ie_j	I/O bit 6 interrupt enable									
85	io5ie_j	I/O bit 5 interrupt enable									
84	io4ie_j	I/O bit 4 interrupt enable									
83	io3ie_j	I/O bit 3 interrupt enable									
82	io2ie_j	I/O bit 2 interrupt enable									
81	io1ie_j	I/O bit 1 interrupt enable									
80	io0ie_j	I/O bit 0 interrupt enable									

FIG. 25

AO-1odmae DMA Enable Register

31

8 7 6 5 4 3 2 1 0

Reserved Zeros											
Bit Address	Mnemonic	Description									
A7	io7dmae_j	I/O bit 7 DMA enable									
A6	io6dmae_j	I/O bit 6 DMA enable									
A5	io5dmae_j	I/O bit 5 DMA enable									
A4	io4dmae_j	I/O bit 4 DMA enable									
A3	io3dmae_j	I/O bit 3 DMA enable									
A2	io2dmae_j	I/O bit 2 DMA enable									
A1	io1dmae_j	I/O bit 1 DMA enable									
A0	io0dmae_j	I/O bit 0 DMA enable									

FIG. 26

CO-vram VRAM Control Bit Register

31

7 6 5 4 3 2 1 0

Reserved Zeros											
Mnemonic	Description										
msvgrp	memory system VRAM group										
dsfvcas	state of <u>DSF</u> at VRAM <u>CAS</u> fall										
dsfvras	state of <u>DSF</u> at next VRAM <u>RAS</u> fall										
casvras	<u>CAS</u> fall before <u>RAS</u> next VRAM <u>RAS</u>										
wevras	<u>LWE</u> low at next VRAM <u>RAS</u> fall										
cevras	<u>OE</u> low at next VRAM <u>RAS</u> fall										

FIG. 27

18/50

E0 misca - Miscellaneous A Register		31	8 7 6 5 4 3 2 1 0
Reserved Zeros			
Mnemonic			Description
mg3rd			memory group 3 refresh disable
mg2rd			memory group 2 refresh disable
mg1rd			memory group 1 refresh disable
mg0rd			memory group 0 refresh disable
mras31d			memory system don't force RAS cycle if A31 = 1
mshacd			memory system high address compare disable
mrtg			memory system refresh timing group

FIG. 28

100 miscb - Miscellaneous B Register		31	8 7 6 5 4 3 2 1 0
Reserved Zeros			
Mnemonic			Description
mmib			multiple memory bank
fdmap			fixed DMA priorities
pkgio			package has VO pins
oed			OE disable
mg3bw			memory group 3 byte wide
mg2bw			memory group 2 byte wide
mg1bw			memory group 1 byte wide
mg0bw			memory group 0 byte wide

FIG. 29

120 mfltaddr - Memory Fault Address Register		31	0
Memory Fault Address			

Register is read-only. Reading mfltaddr after a memory fault releases the data lock on mfltaddr and mfltdata, allowing data to flow into the registers.

FIG. 30

19/50

140 mftdata Memory Fault Data Register

31

0

Memory Fault Data

Register is read-only. Reading mftaddr after a memory fault releases the data lock on mftaddr and mftdata, allowing data to flow into the registers.

FIG. 31

160 msgam Memory System Group Select Mask Register

31

16 15

0

Reserved Zeros**Memory System Group-Select Mask**

Contains zero, one, or two adjacent bits to determine which, if any, of the upper 16 address bits will be decoded to select memory groups.

FIG. 32

180 mgds Memory Group Device Size Register

31

16 15

12 11

8 7

4 3

0

Reserved Zeros**Mnemonic****Description**

mg3ds memory group 3 device size

mg2ds memory group 2 device size

mg1ds memory group 1 device size

mg0ds memory group 0 device size

Device Sizes

0x00	64K DRAM	0x04	1M DRAM	0x08	8M DRAM	0x0c	64M DRAM (asym)
0x01	128K DRAM	0x05	2M DRAM	0x09	16M DRAM (asym)	0x0d	64M DRAM
0x02	256K DRAM	0x06	4M DRAM (asym)	0x0a	16M DRAM	0x0e	128M DRAM
0x03	512K DRAM	0x07	4M DRAM	0x0b	32M DRAM	0x0f	SRAM

FIG. 33

20/50

1AO misc0 Miscellaneous C Register

31	8 7 6 5 4 3 0
	Reserved Zeros
Mnemonic	Description
pkgmfit	package has memory fault pin
mspwe	memory system posted-write enable
msexvhacr	memory system exclude VRAM from high address compare RAS cycles
msexxa31hac	memory system exclude A31 from high address compare
msbsa	memory system SRAM bank select offset from A14 (A12 for byte mode) to the two bits for SRAM bank select (0-9 valid, 0xa-0xf invalid)

FIG. 34

mgXebt: Memory Group 0-3 Extended Bus Timing Registers

1C0 mg0ebt 1E0 mg1ebt 200 mg2ebt 220 mg3ebt

31	11 10	8 5	2 1 0
	Reserved Zeros		
Mnemonic	Description		
mgebtsum	memory group extended bus timing sum (0, 1, 2, ..., 31) 2X-clocks		
mgebtddoe	memory group extended bus timing <u>DD8</u> expansion (0, 1, 2, ..., 15) 2X-clocks		
mgebtcase	memory group extended bus timing <u>CAS</u> extension (0, 1, 2, 4) 2X-clocks		

FIG. 35

21/50

mgXcasbt Memory Group 0-3 CAS Bus Timing Registers

240 mg0casbt 260 mg1casbt 280 mg2casbt 2A0 mg3casbt

31 16 15 13 12 9 8 4 3 2 1 0

Reserved Zeros											
Mnemonic	Description										
mgbtcas	memory group bus timing <u>CAS</u> low start (1, 2, 3, ..., 8) 4X-clock cycles										
mgbtdob	memory group bus timing <u>DOB</u> low start (1, 2, 3, ..., 16) 4X-clock cycles										
mgbtcast	memory group bus timing <u>CAS</u> cycle total (1, 2, 3, ..., 32) 2X-clock cycles										
mgbtwea	memory group bus timing late fall <u>EWE</u> active (0=active at cycle start, 1=active at <u>CAS</u> low)										
mgbtwea	memory group bus timing <u>EWE</u> active, delay by one 4X-clock cycle										
mgbtceo	memory group bus timing early rise <u>OE</u> by one 4X-clock cycle										
mgbtewe	memory group bus timing early rise write enables by one 4X-clock cycle										

FIG. 36

mgXrasbt Memory Group 0-3 RAS Bus Timing Registers

2C0 mg0rasbt 2E0 mg1rasbt 300 mg2rasbt 320 mg3rasbt

31 13 9 8 5 4 1 0

Reserved Zeros							
Mnemonic	Description						
mgbtrast	memory group bus timing RAS prefix cycle total + 1 (0, 1, 2, ..., 31) 2X-clock cycles						
mgbtras	memory group bus timing <u>RAS</u> low start (1, 2, 3, ..., 16) 2X-clock cycles						
mgbthid	memory group bus timing row address hold (0, 1, 2, ..., 15) 2X-clock cycles						
mgbteras	memory group bus timing early <u>RAS</u> low by one 4X-clock cycle						

FIG. 37

22/50

IoXebt I/O Channel 0-7 Extended Bus Timing Registers					
340 Io0ebt	360 Io1ebt	380 Io2ebt	3A0 Io3ebt	3C0 Io4ebt	3E0 Io5ebt
3E0 Io6ebt	400 Io7ebt	420 Io8ebt			
31			11 10	6 5	2 1 0
Reserved Zeros					
Mnemonic	Description				
Ioebtsum	I/O channel extended bus timing sum (0, 1, 2, ..., 31 2X-clock cycles)				
Ioebtdobe	I/O channel extended bus timing -DOB expansion (0, 1, 2, ..., 15 2X-clock cycles)				
Ioebtcase	I/O channel extended bus timing -CAS extension (0, 1, 2, 4 2X-clock cycles)				

FIG. 38

440 msra Memory System Refresh Address					
WRITE ONLY					
31 30	22 21	18 15		2 1 0	
Reserved					
				0 0	
Mnemonic	Description				
msra	memory system RAS refresh addr on AD[24:11]				
msrah	memory system refresh high address on AD[30:25]				
msra31	memory system refresh address on AD31				

FIG. 39

440 Iopdelay IOP Delay Counter Register					
READ ONLY					
31				0	
IOP Delay Counter					

FIG. 40

23/50

480 lodtt a I/O Device Transfer Types A Register

31

8 7 6 5 4 3 2 1 0

Reserved Zeros

	Mnemonic	Description
Device Transfer Types	io3dtt	DMA channel 3 device transfer type
0 four-byte bye-transfer	io2dtt	DMA channel 2 device transfer type
1 one-byte byte-transfer	io1dtt	DMA channel 1 device transfer type
2 one-cell cell-transfer	io0dtt	DMA channel 0 device transfer type
3 illegal		

FIG. 41

480 lodtt b I/O Device Transfer Types B Register

31

8 7 6 5 4 3 2 1 0

Reserved Zeros

	Mnemonic	Description
Device Transfer Types	io7dtt	DMA channel 7 device transfer type
0 four-byte bye-transfer	io6dtt	DMA channel 6 device transfer type
1 one-byte byte-transfer	io5dtt	DMA channel 5 device transfer type
2 one-cell cell-transfer	io4dtt	DMA channel 4 device transfer type
3 illegal		

FIG. 42

Reserved Register Addresses

4A0-780

FIG. 43

24/50

7AO Iodmaex DMA Enable Expiration Register

31

8 7 6 5 4 3 2 1 0

Reserved

Mnemonic

io7dmaex	I/O bit 7 DMA enable expiration
io6dmaex	I/O bit 6 DMA enable expiration
io5dmaex	I/O bit 5 DMA enable expiration
io4dmaex	I/O bit 4 DMA enable expiration
io3dmaex	I/O bit 3 DMA enable expiration
io2dmaex	I/O bit 2 DMA enable expiration
io1dmaex	I/O bit 1 DMA enable expiration
io0dmaex	I/O bit 0 DMA enable expiration

Description

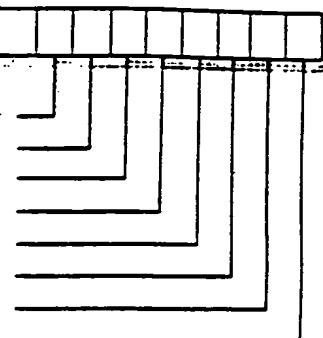


FIG. 44

7CO drivers Driver Current Register

31 29 28 26 25 23 22 20 19 18 17 16 15

0

Reserved

Mnemonic

outdrv	bit output pin drive
rasbcasbdrv	RAS, CAS pin drive
ctrbdrv	control B pin drive (RAS, DQ, DSR)
baniodrv	MGSx/RASx, CASx pin drive
ctriadrv	control A pin drive (OE, EWE, LWE, CAS)
addrv	AD pin drive

Description

3-Bit Field	2-Bit Field	Where n =
00n 1 of 3 drivers	On 1 of 3 drivers	0 1 of 2 pre-drivers
01n 2 of 3 drivers	1n 3 of 3 drivers	1 2 of 2 pre-drivers
11n 3 of 3 drivers		

FIG. 45

7EO Iopreset IOP Reset Register

31

0

write reset IOP on any write
 read 0xffffffff while waiting to reset, zero otherwise

FIG. 46

25/52

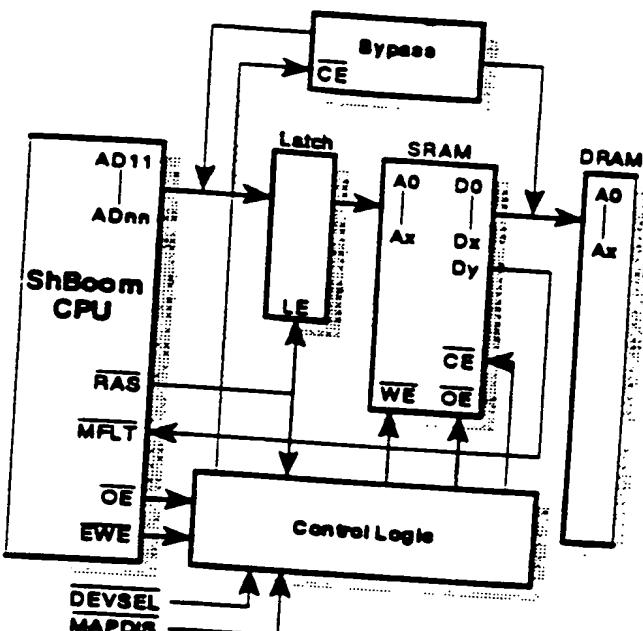
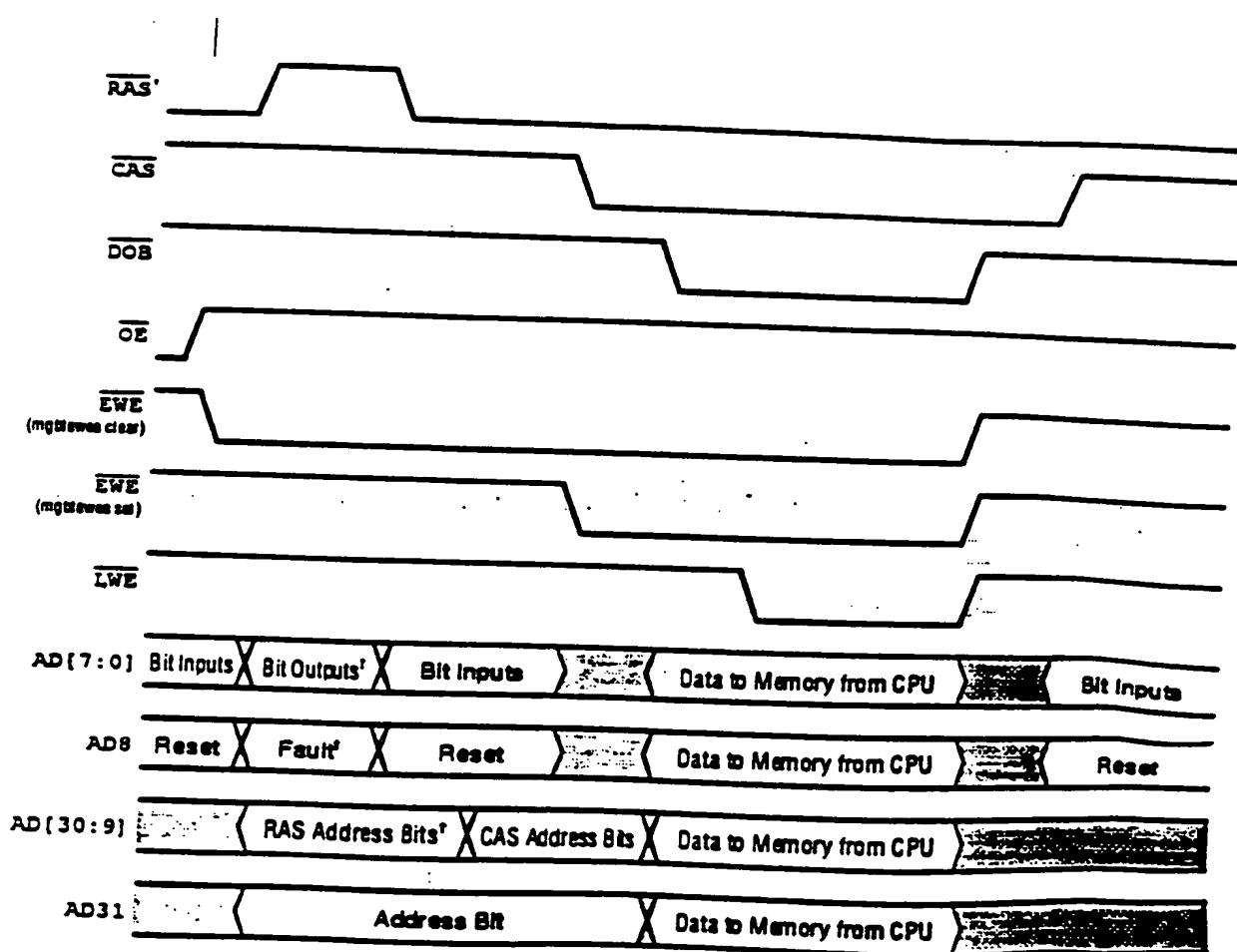


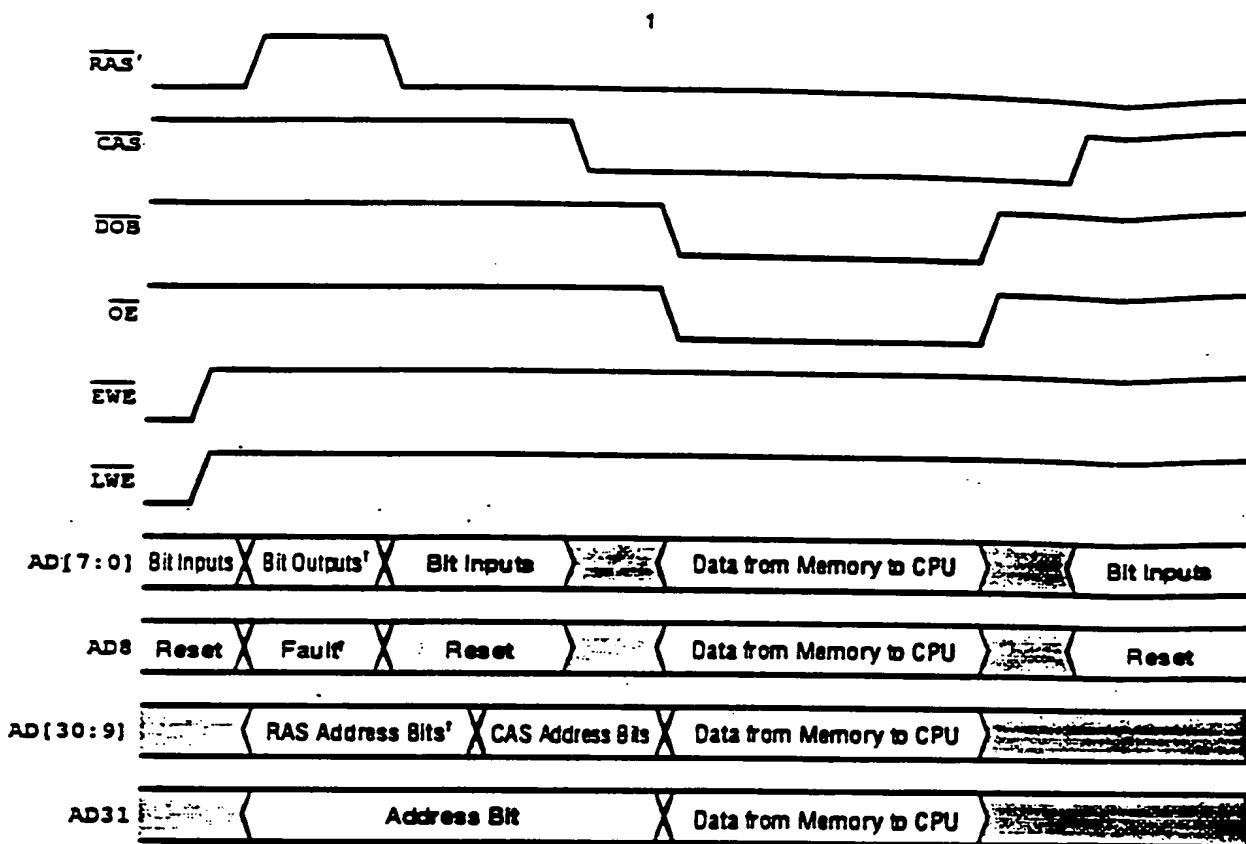
FIG. 46a

FIG. 47



† Presence of XA3 inactive period depends on system conditions.

26/50



F16 48

27/50

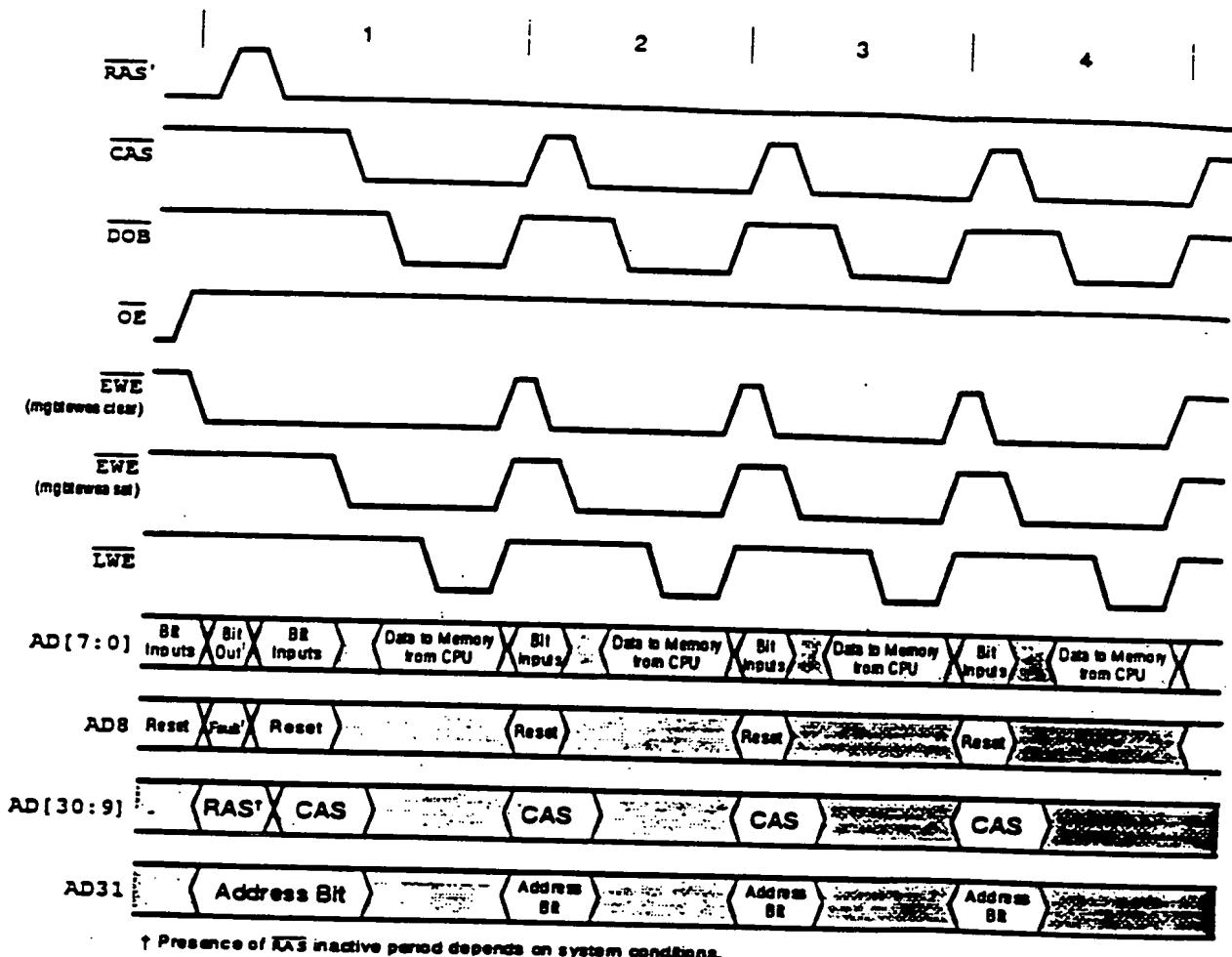


FIG. 49

28/50

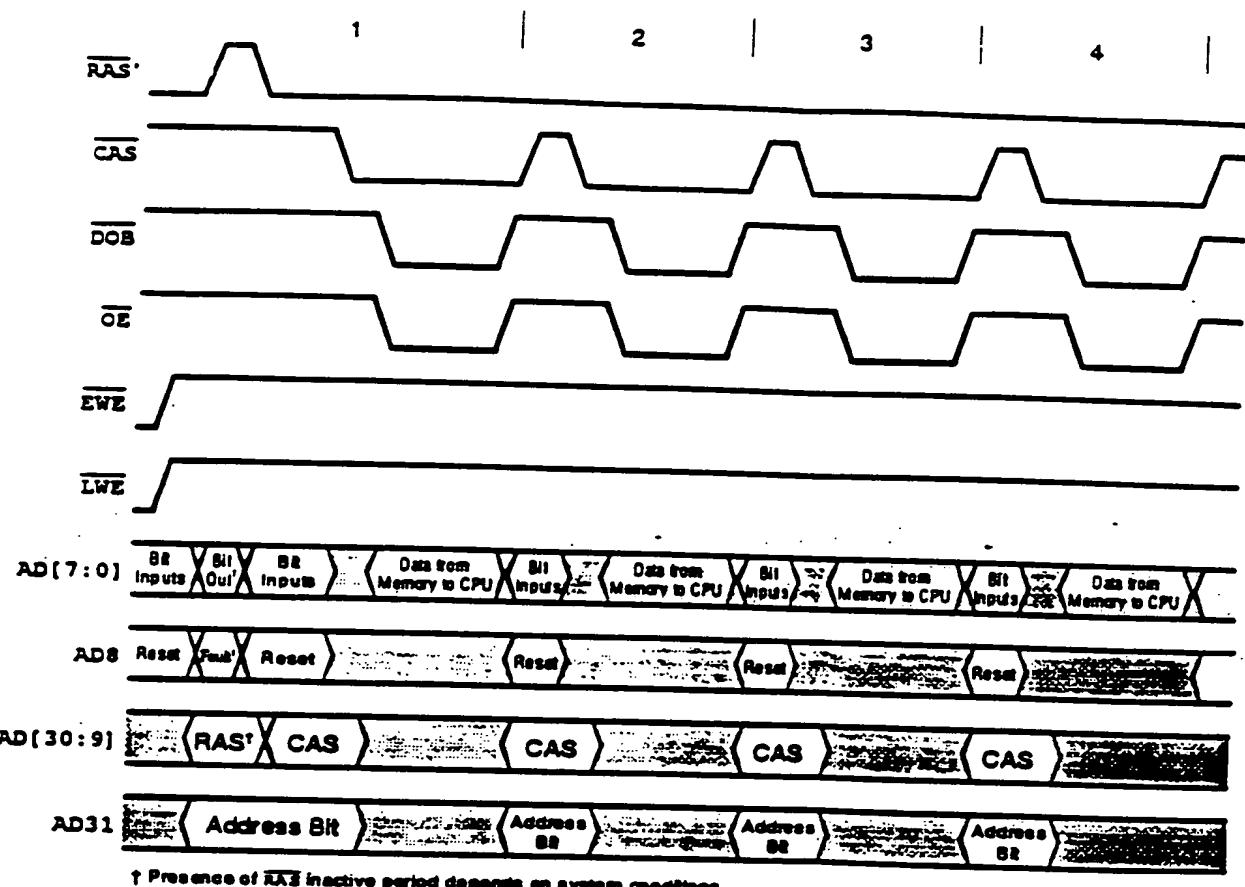
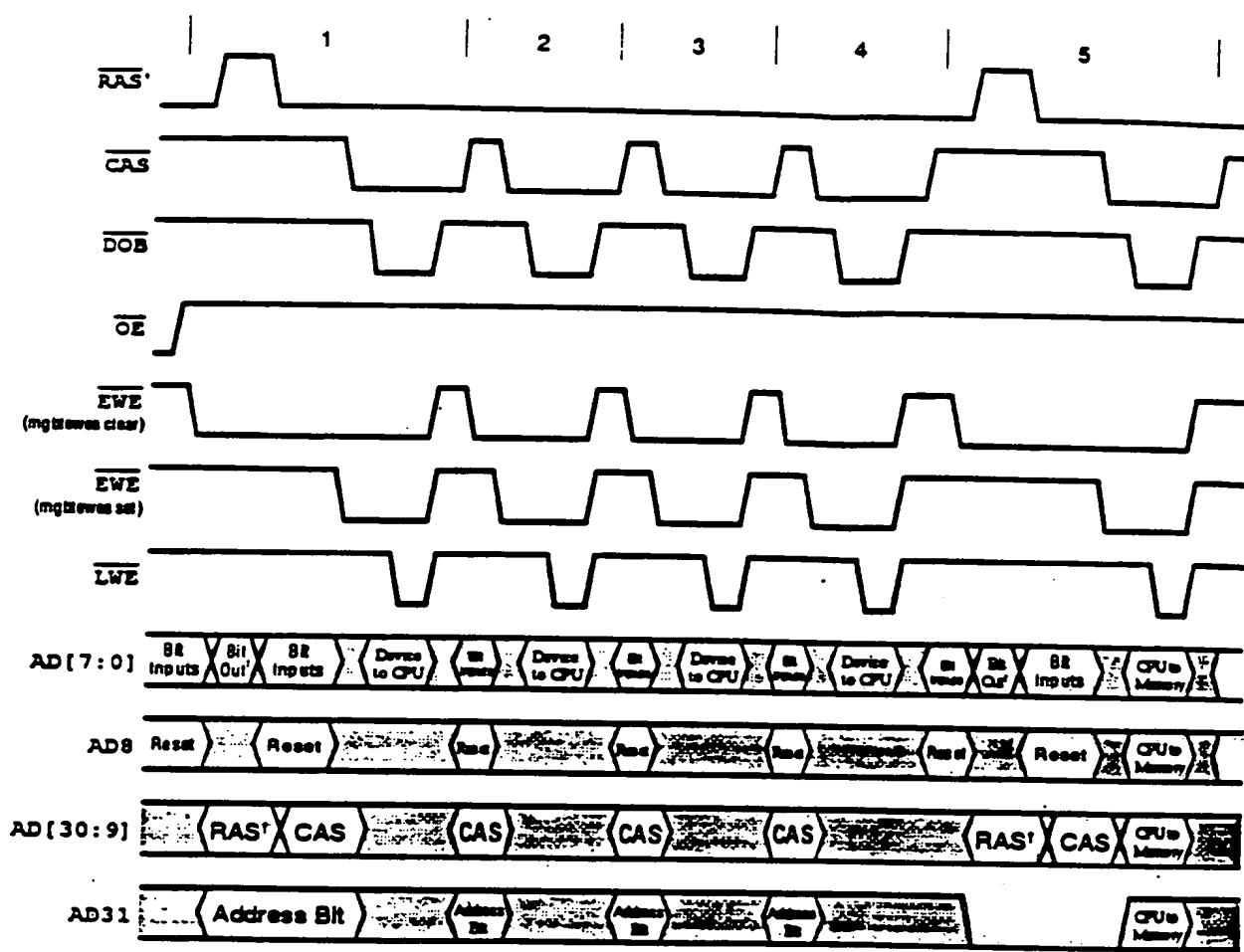


FIG. 50

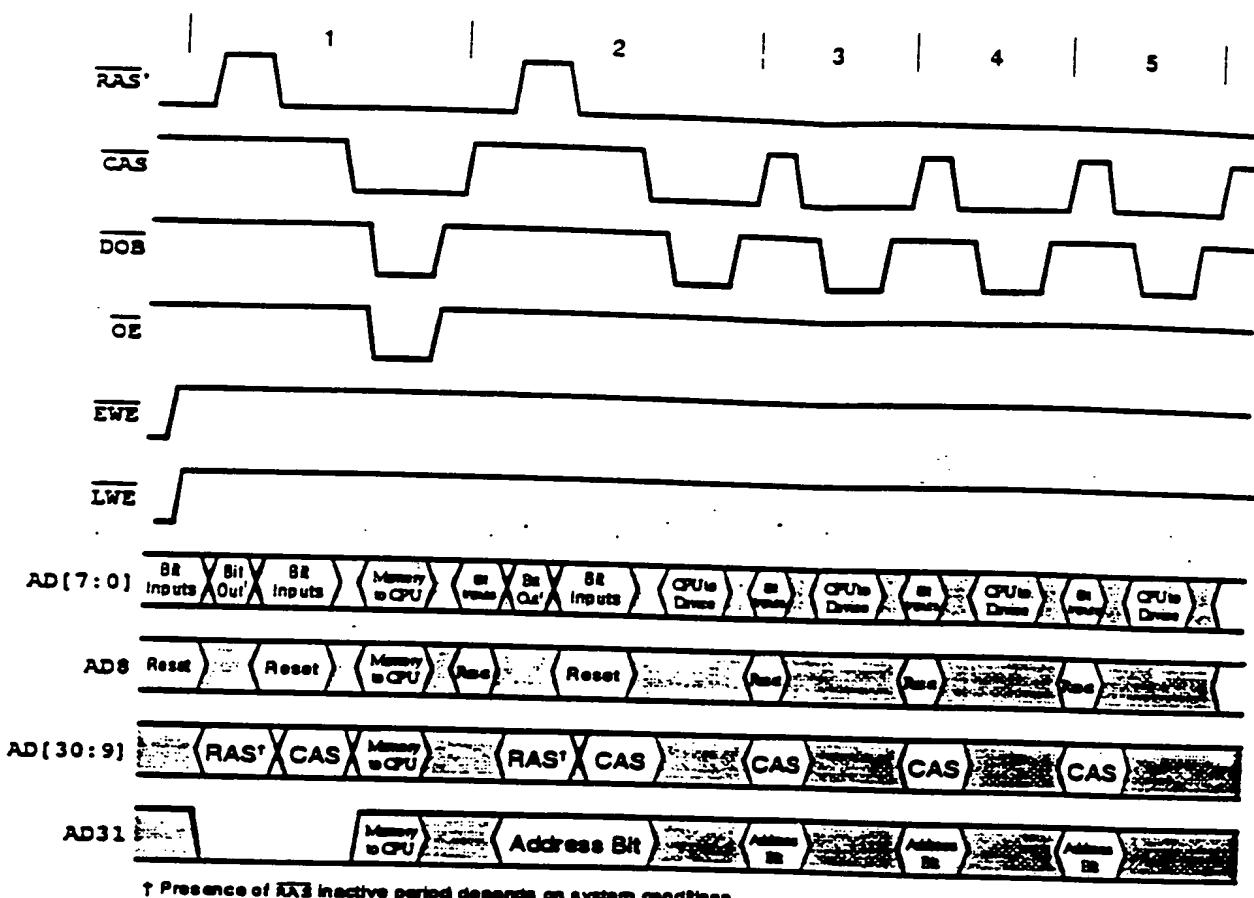
29/50



† Presence of ~~RAS~~ inactive period depends on system conditions.

Fig. 51

30/50



F/6. 52

31/50

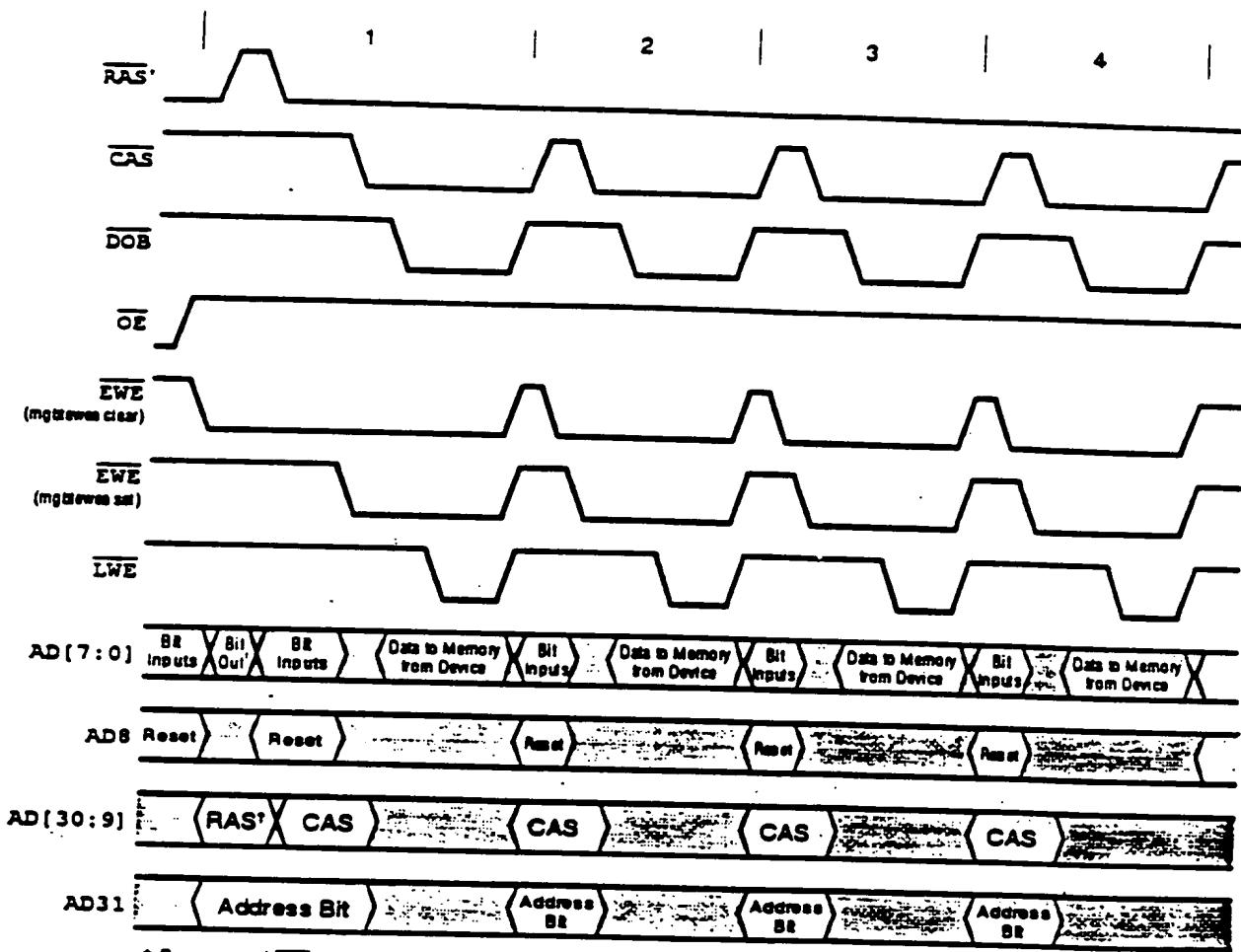


FIG. 53

32/50

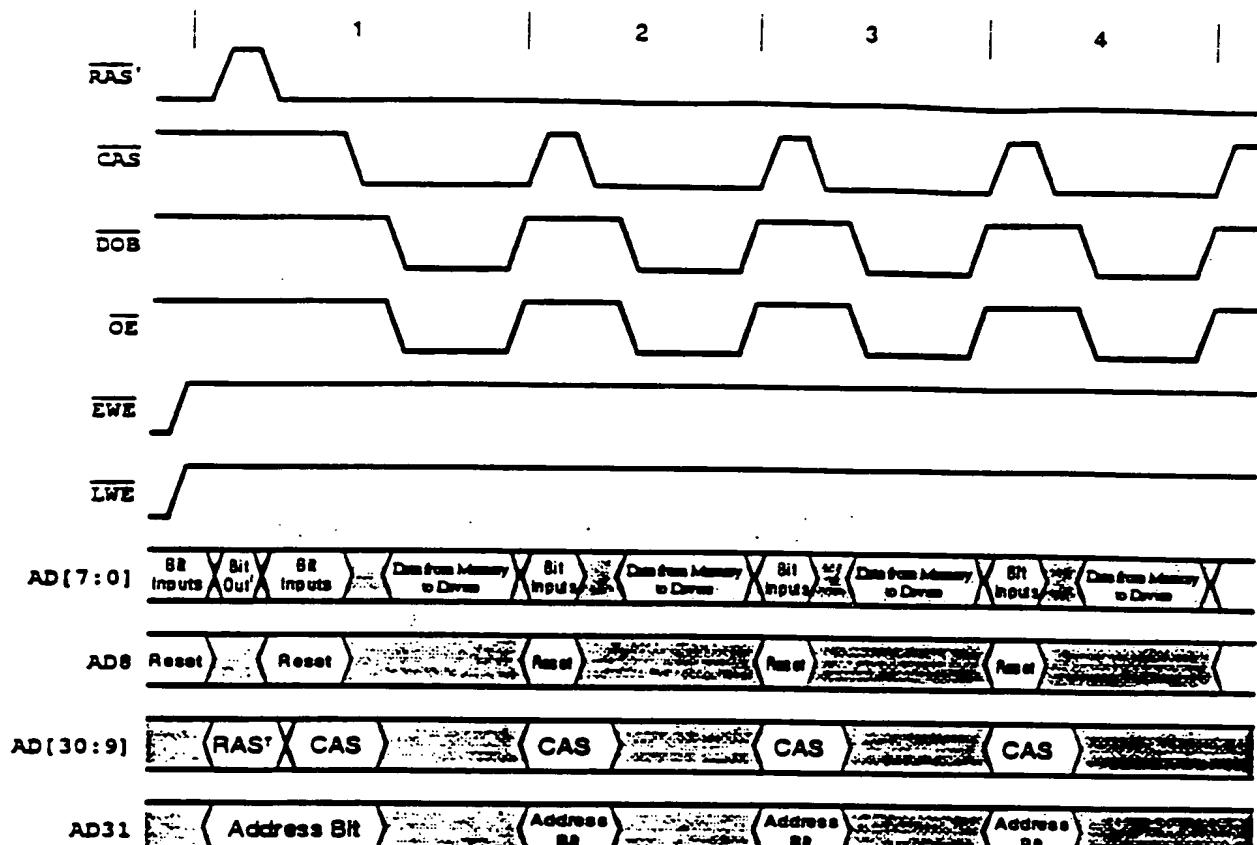


FIG. 54

33/50

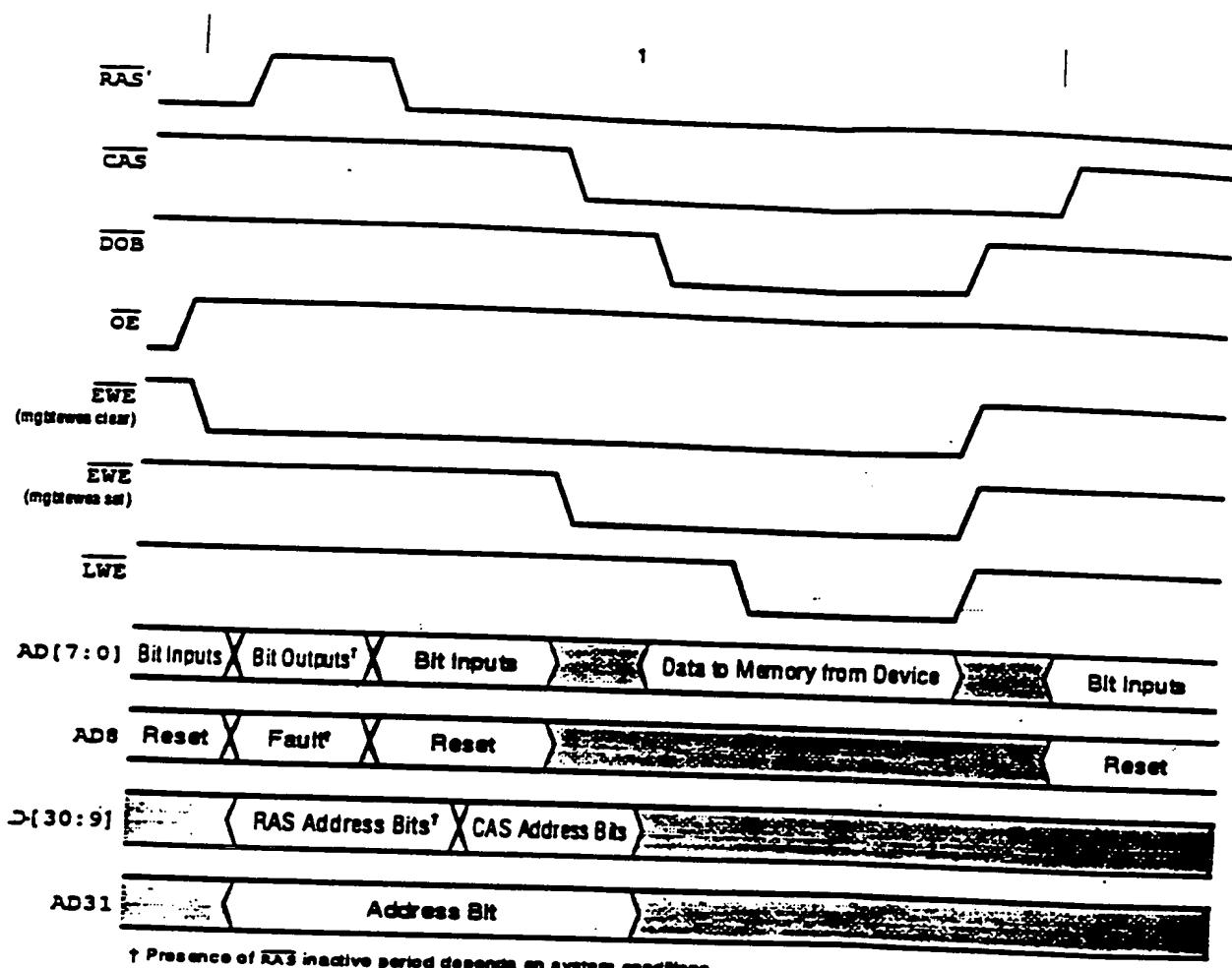


FIG. 55

34/50

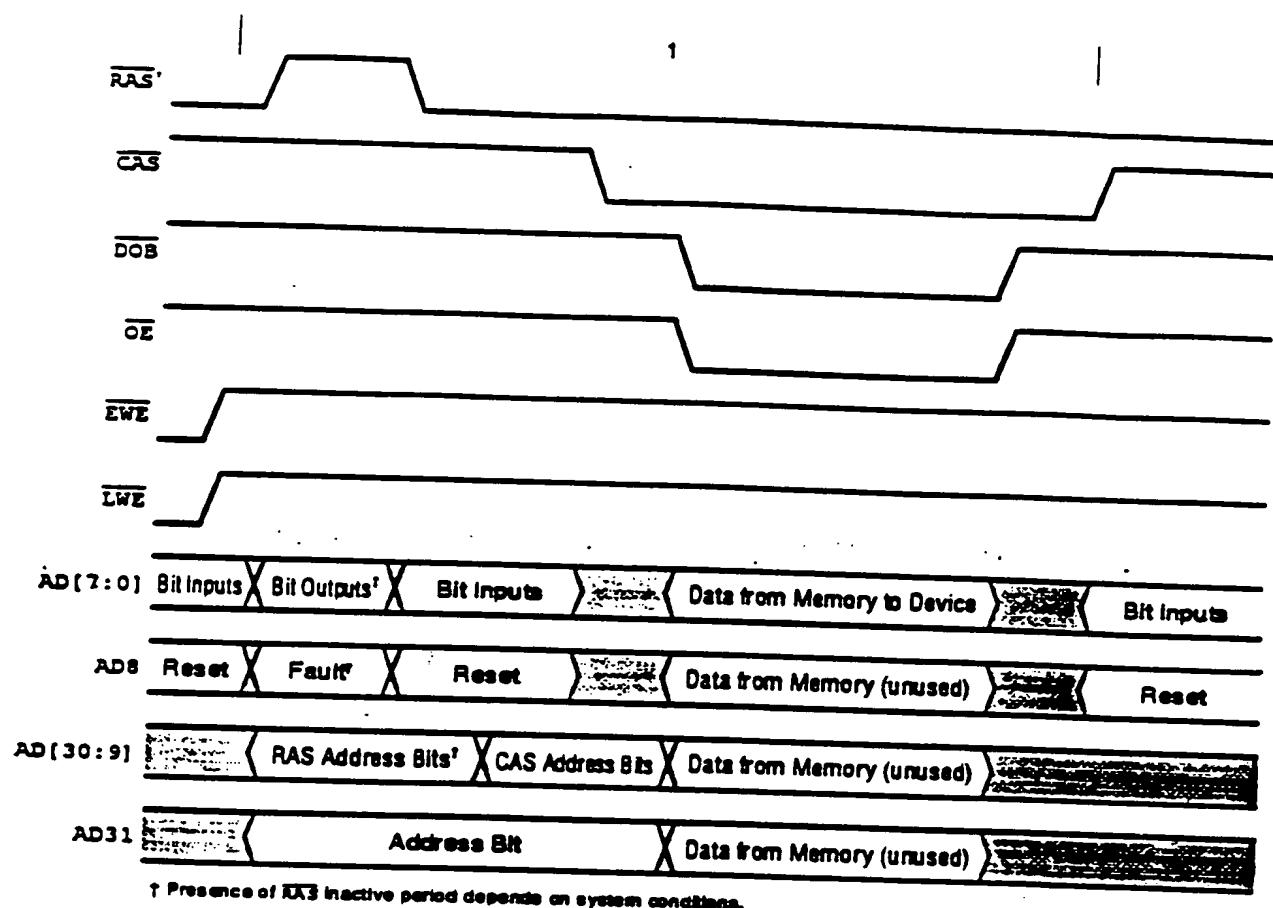


Fig. 56

35/50

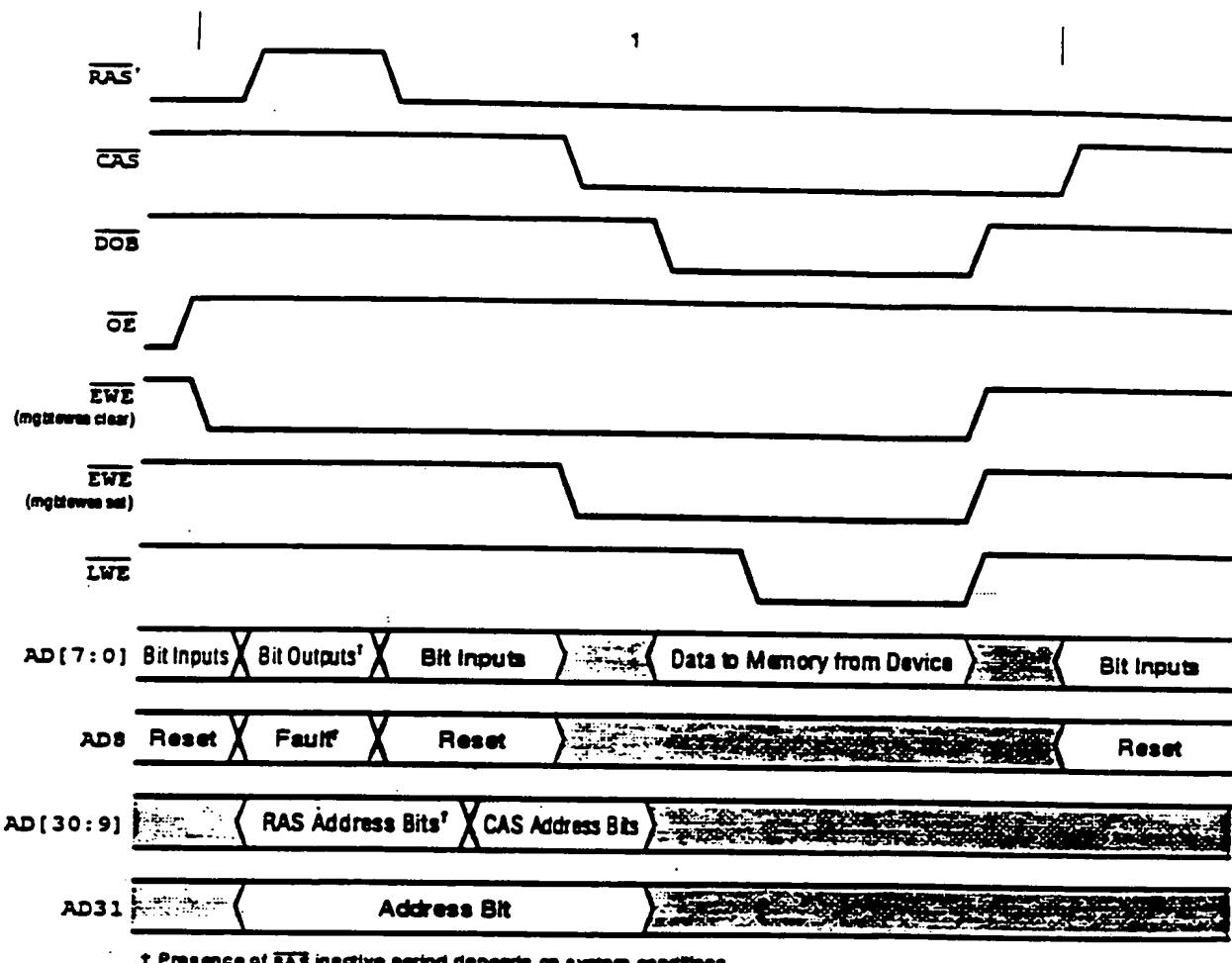


FIG. 57

36/50

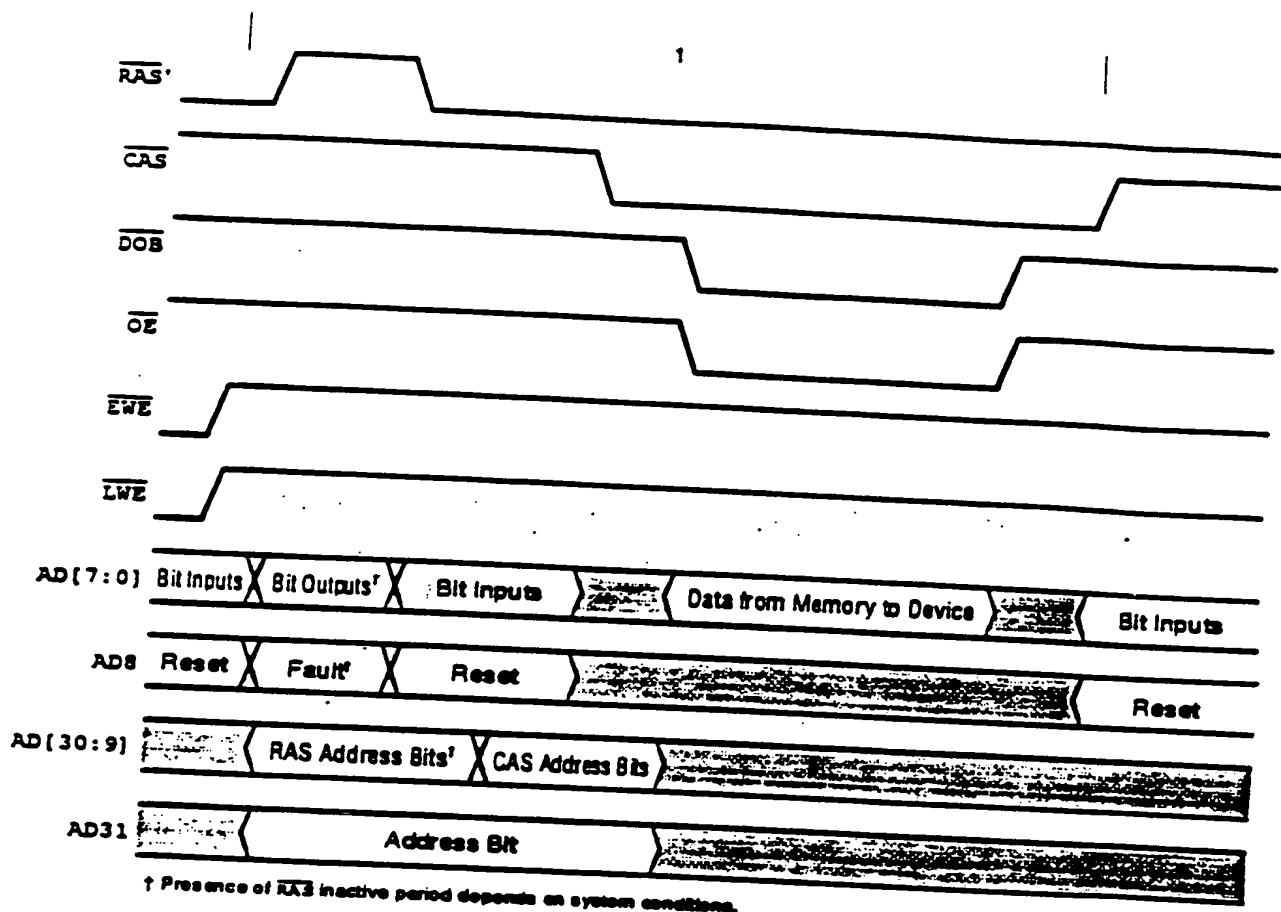


Fig. 58

37/50

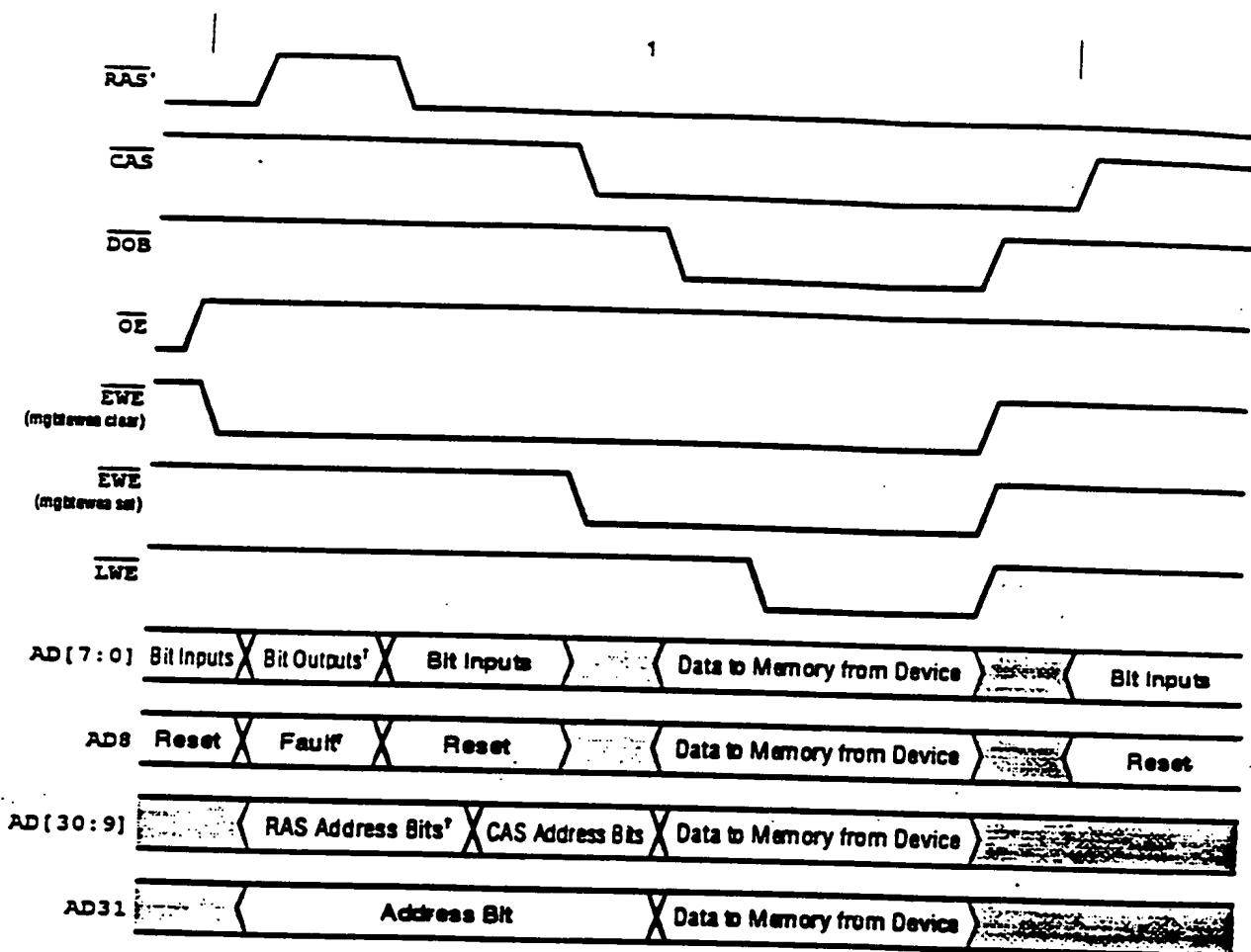


FIG. 59

38/50

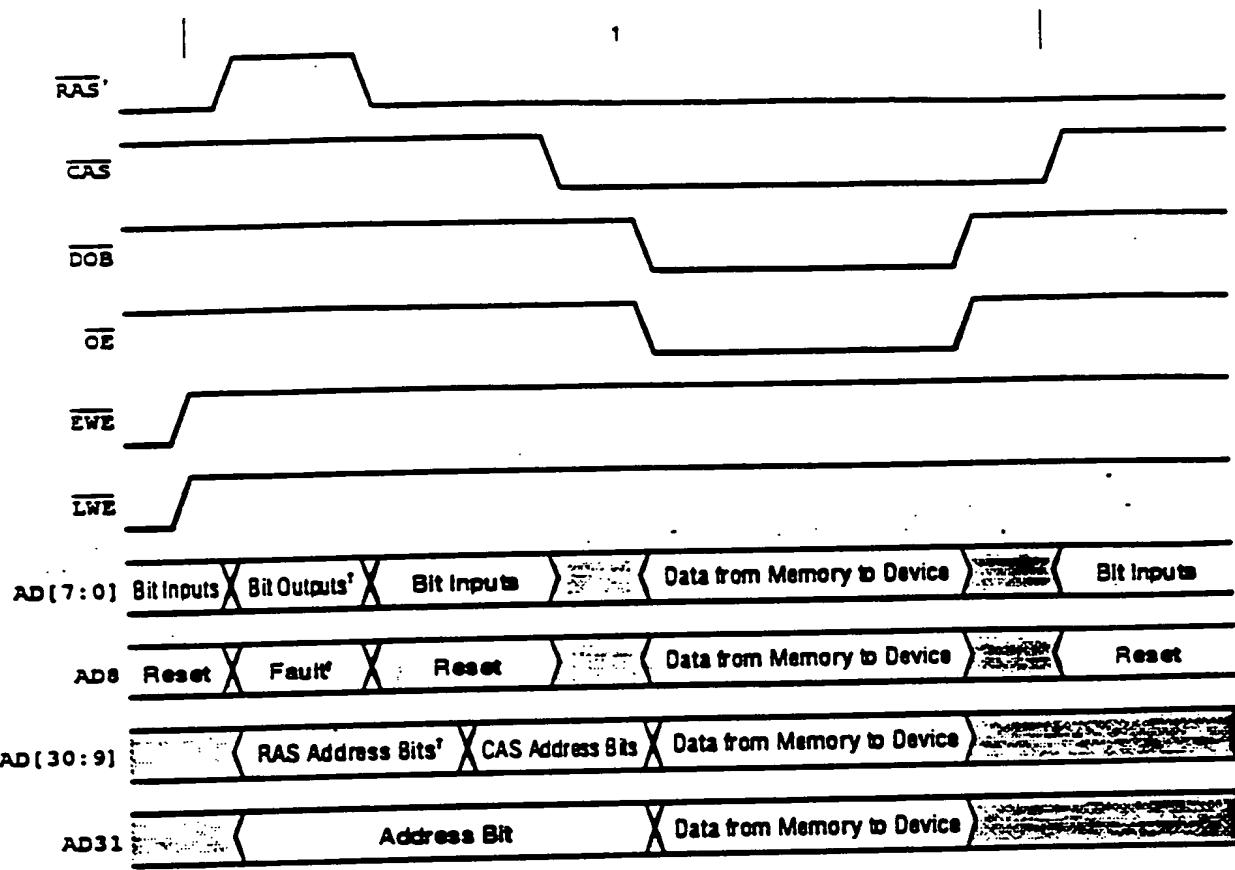


Fig. 60

39/50

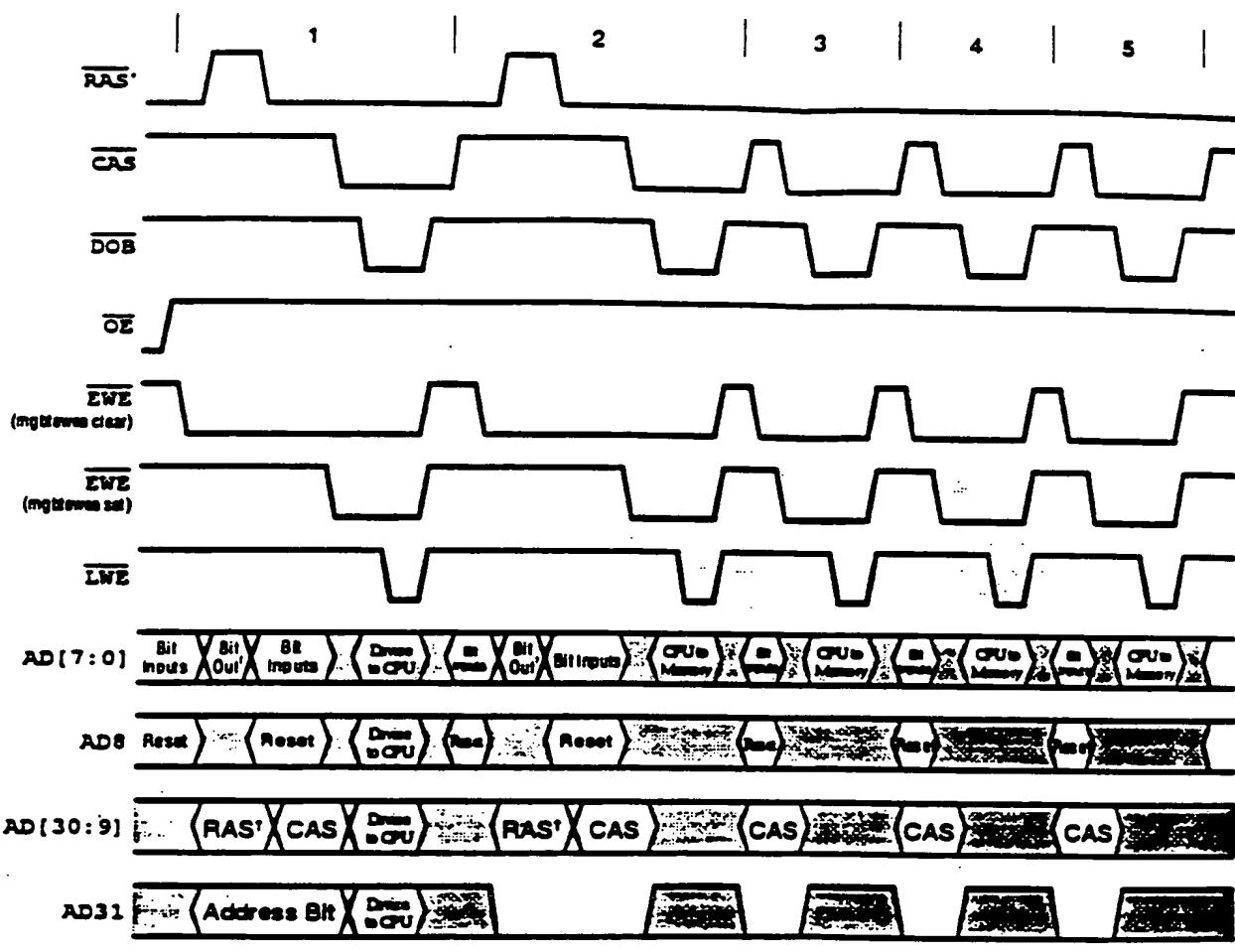


FIG. 61

40/50

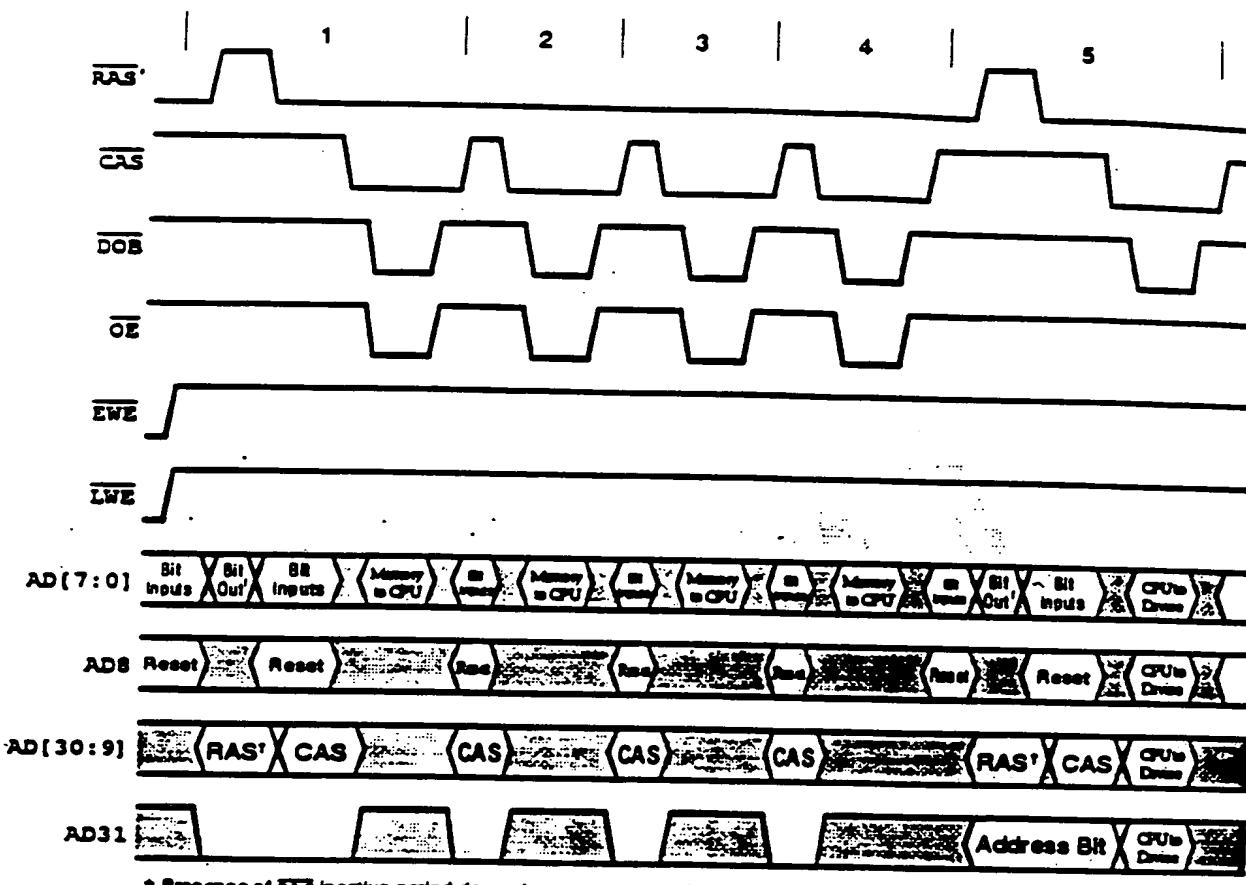
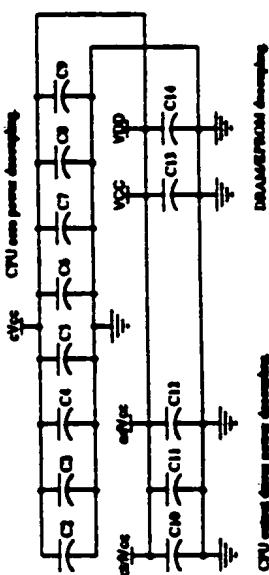
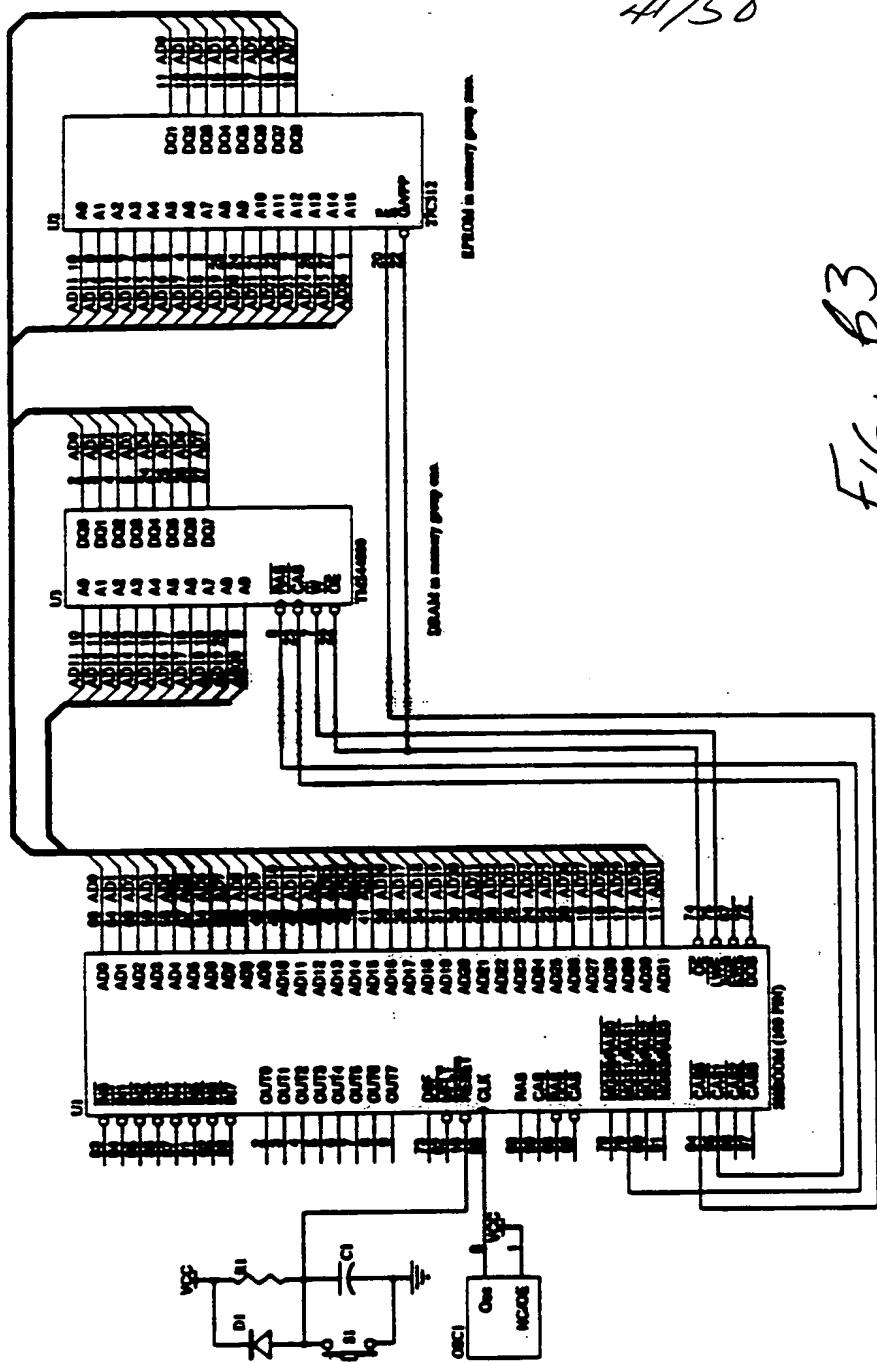


Fig. 62

44/50

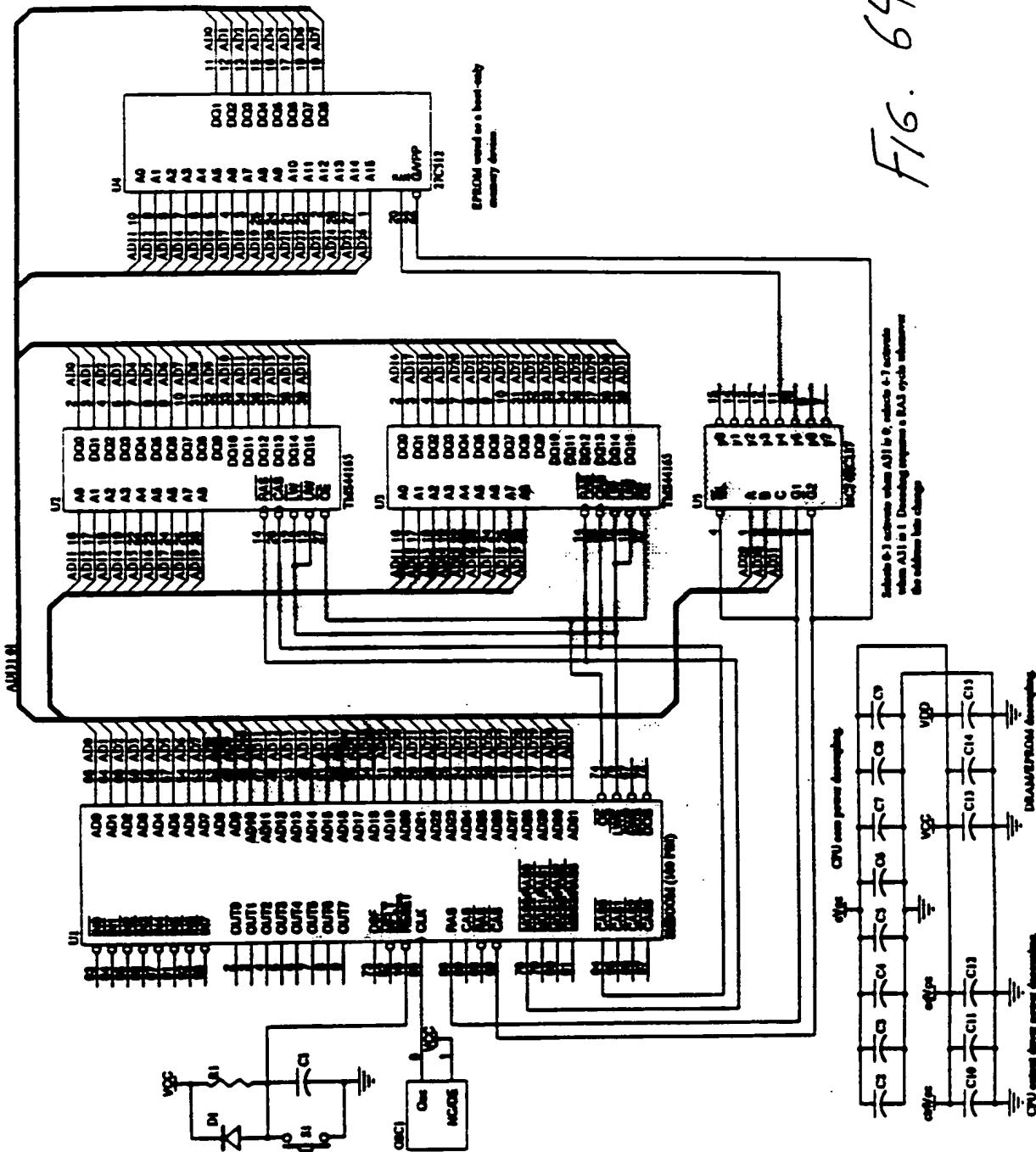
Fig. 63



0905122639 0920236

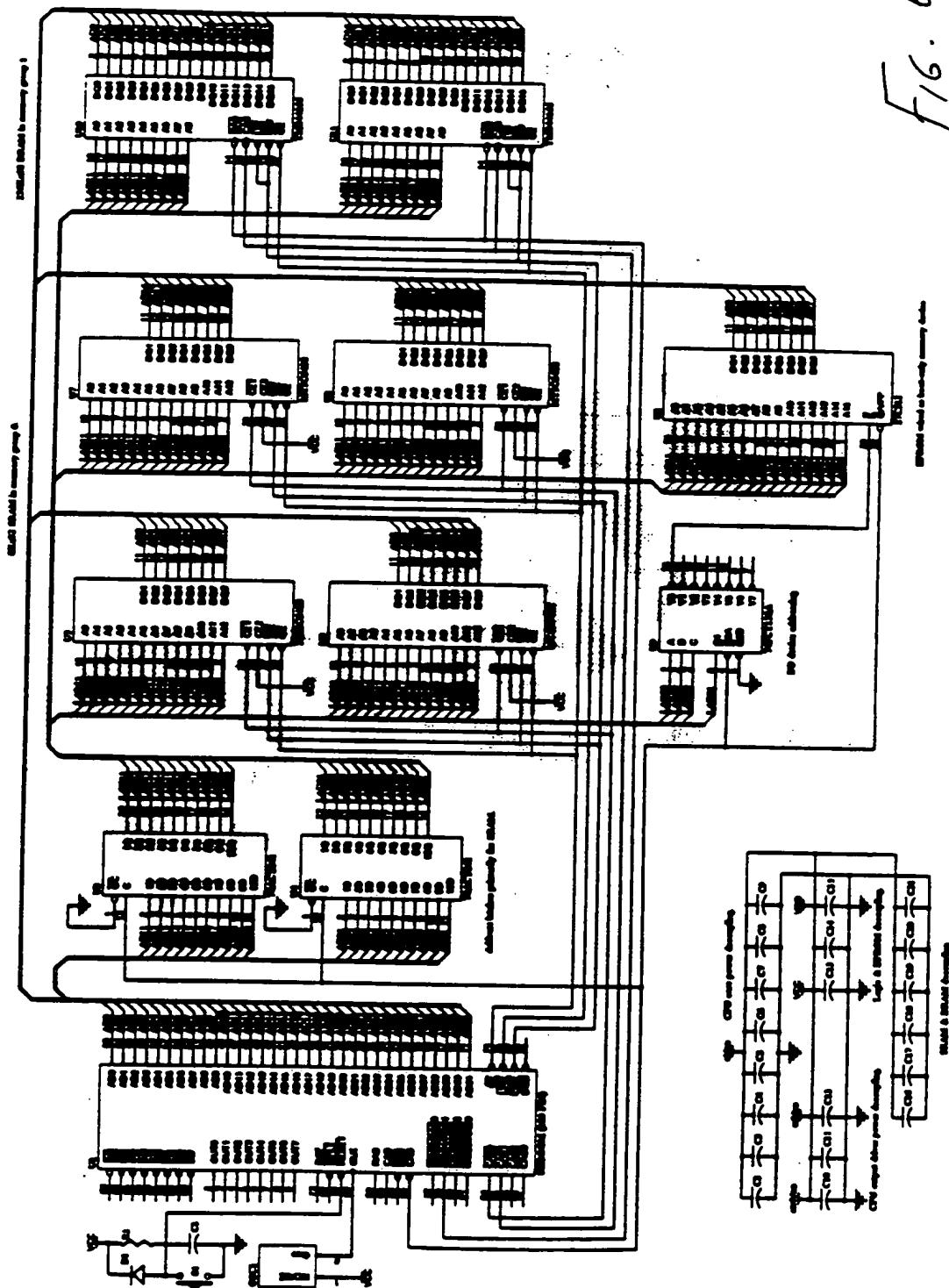
42/50

Fig. 64.



43/50

Fig. 65



44/50

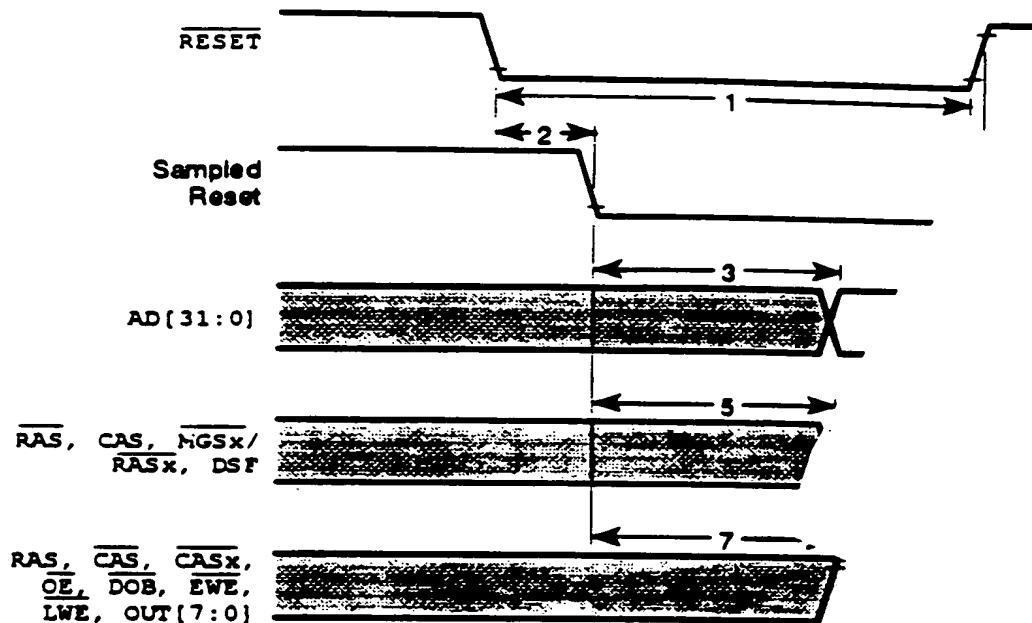


FIG. 66

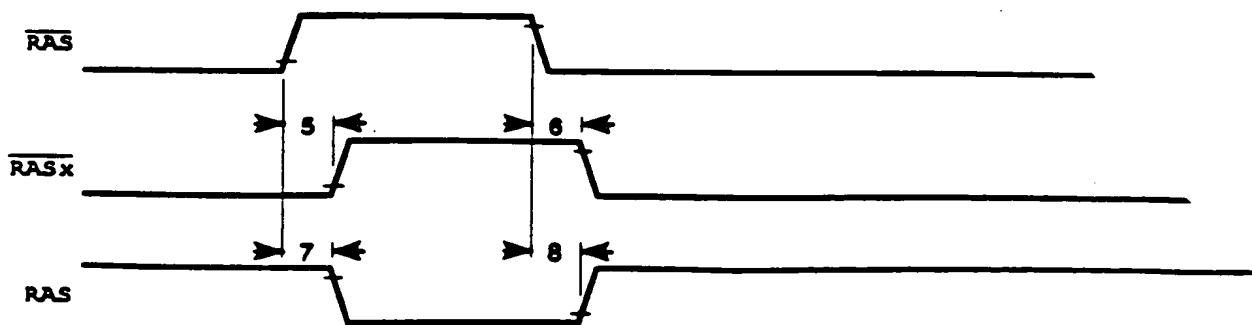
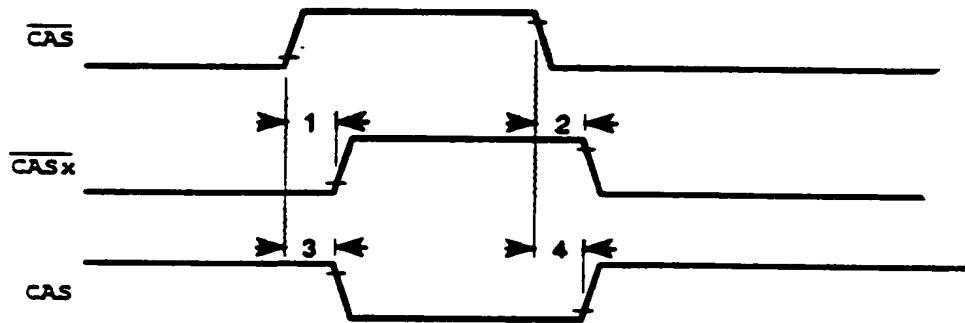


FIG. 69

45/50

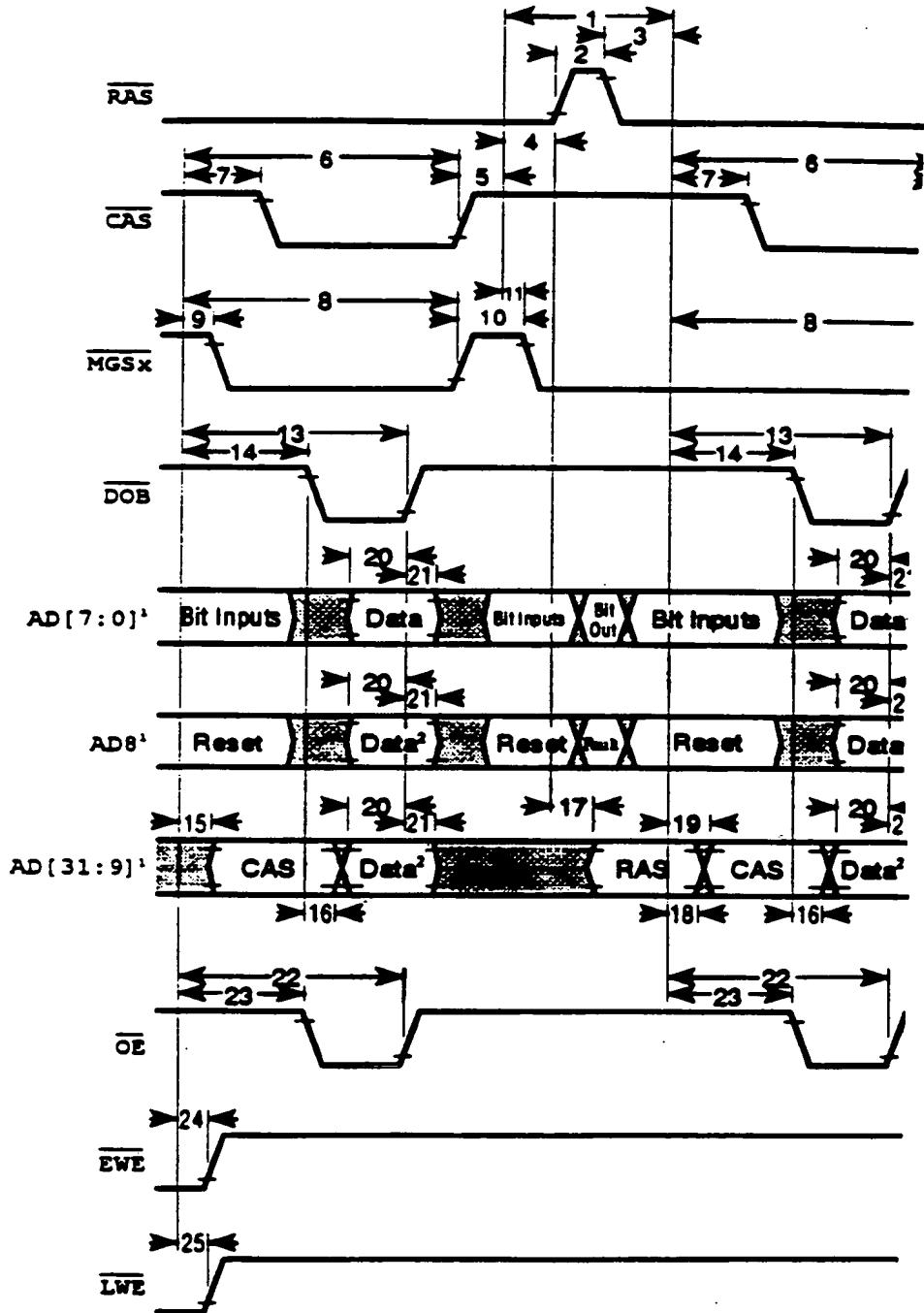


FIG. 67

46/50

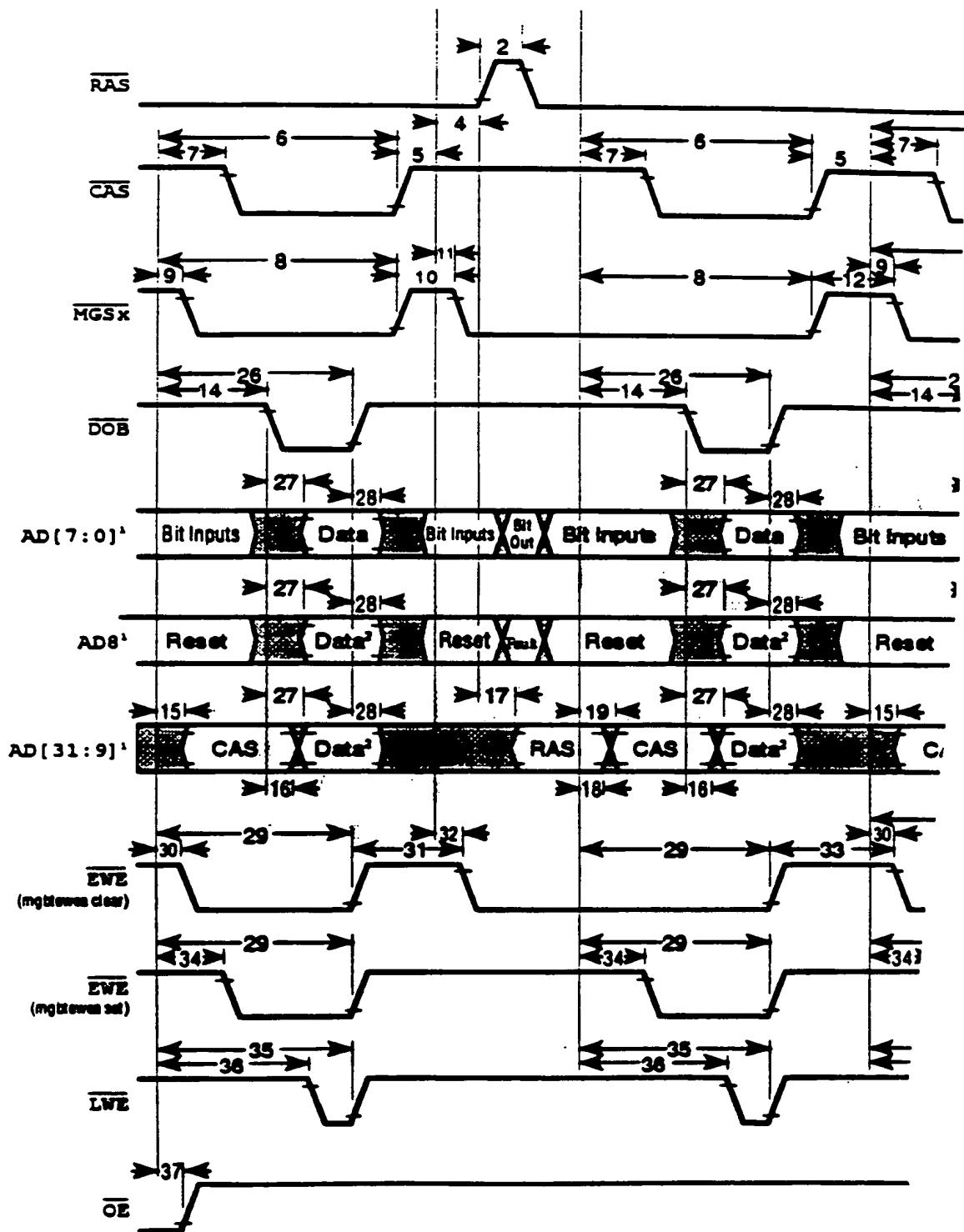


FIG. 68

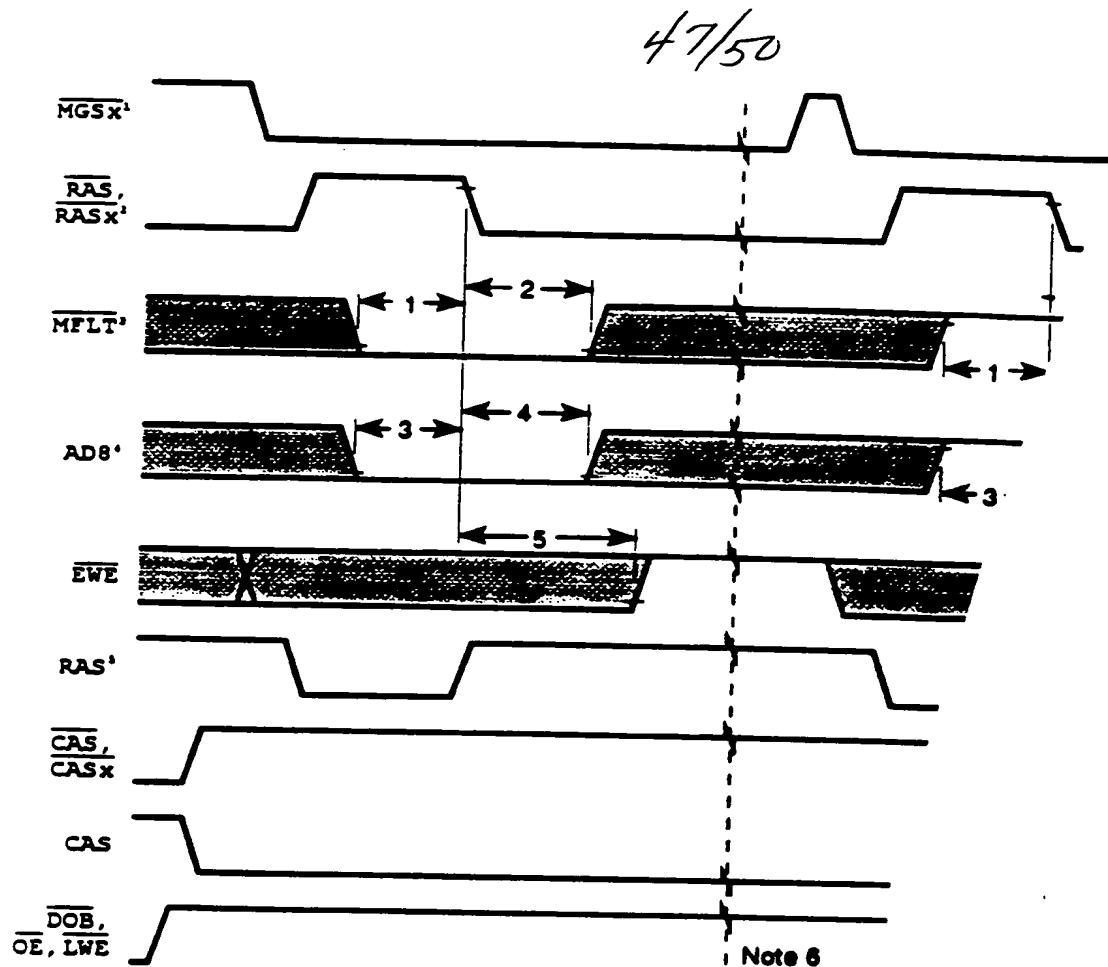


FIG. 70

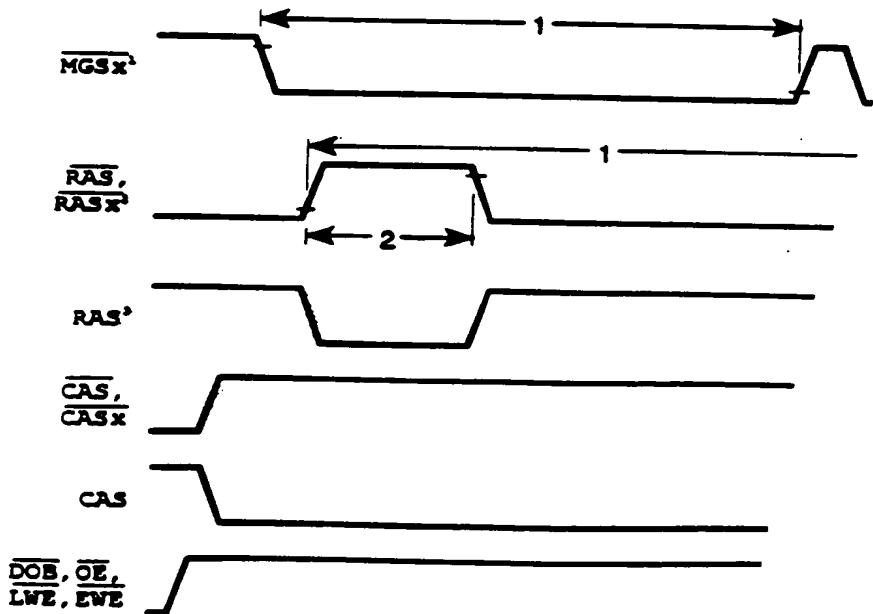


FIG. 71

48/50

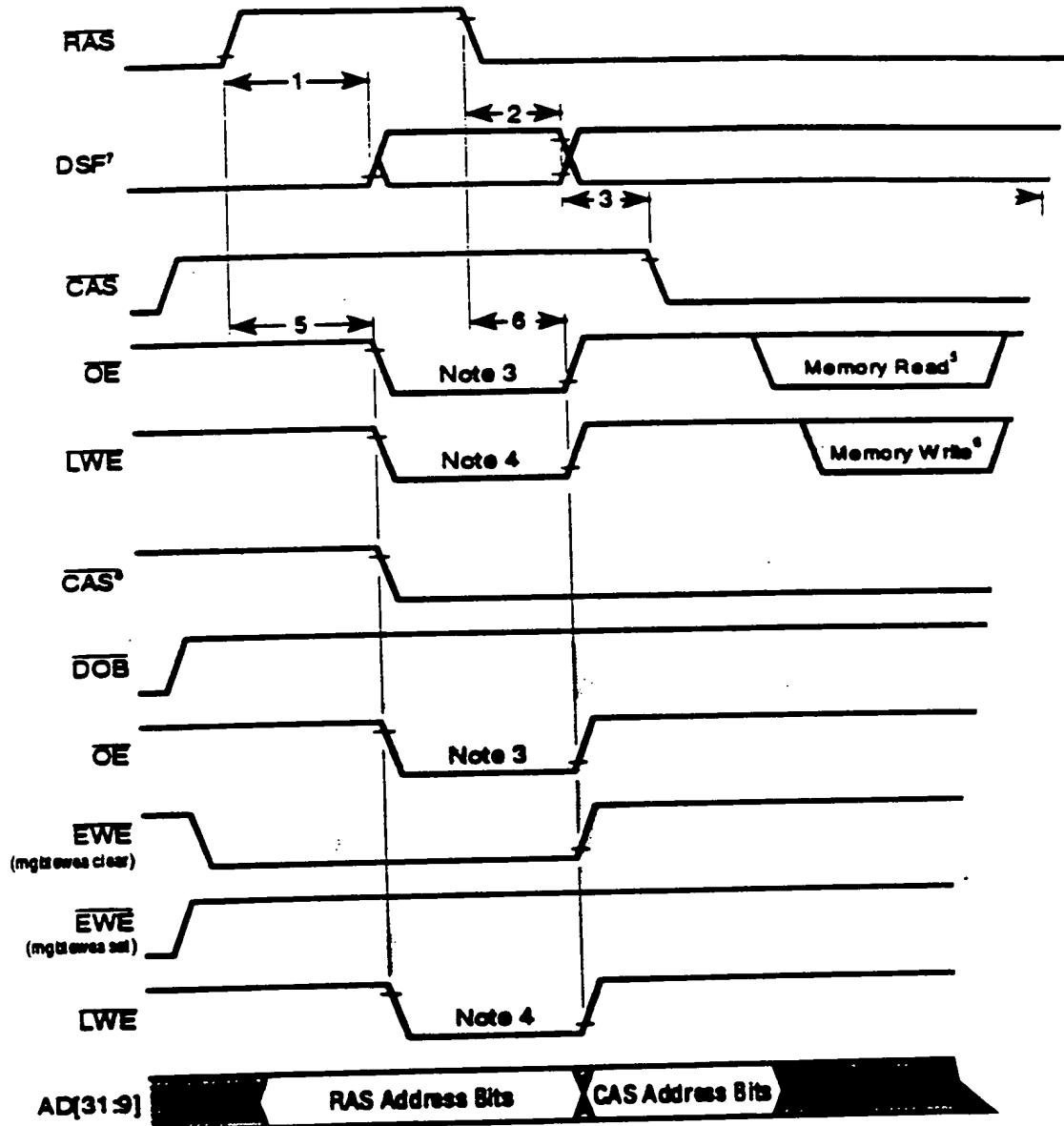


FIG. 72

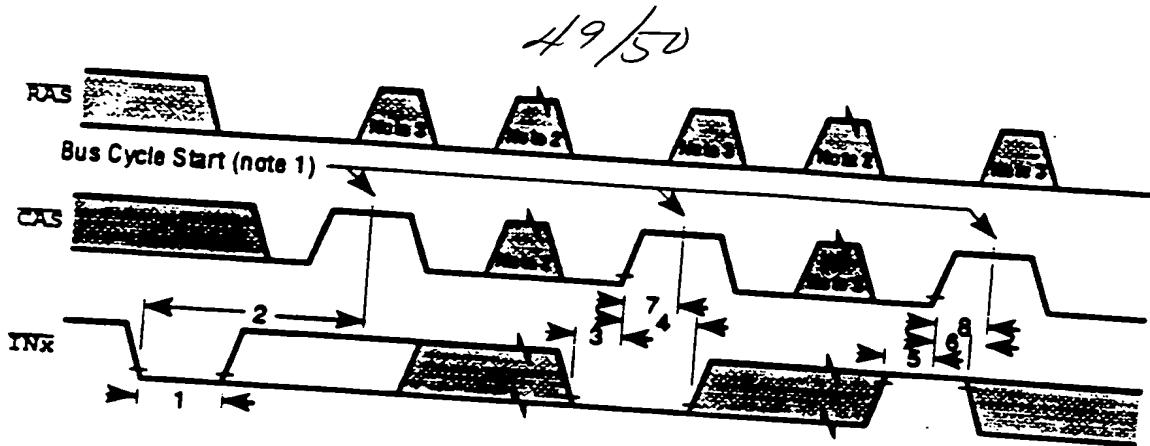


FIG. 73

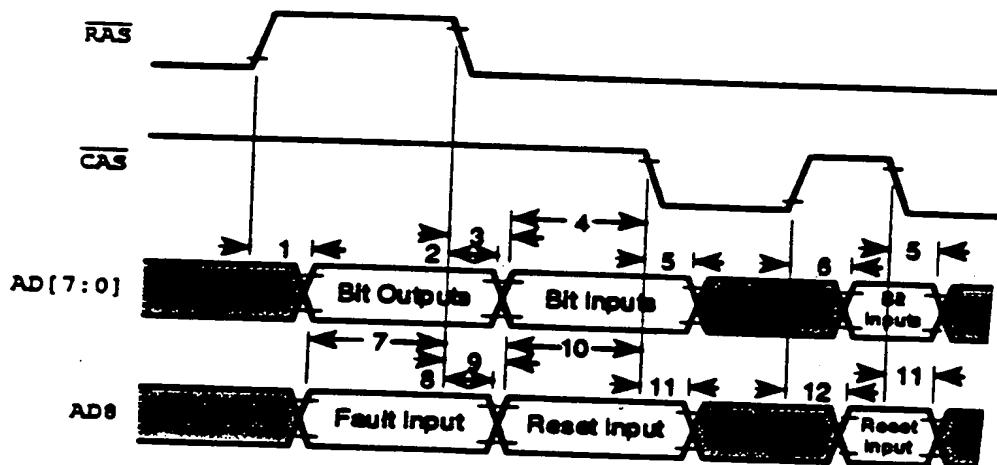


FIG. 74

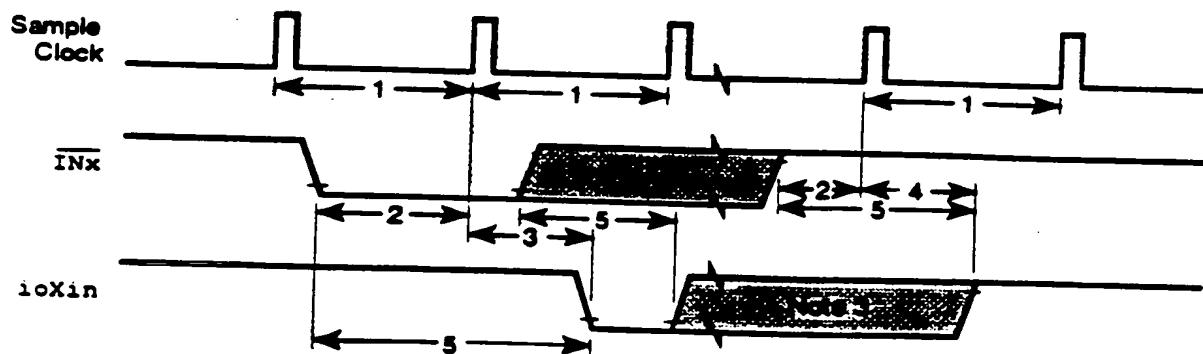


FIG. 75

50/50

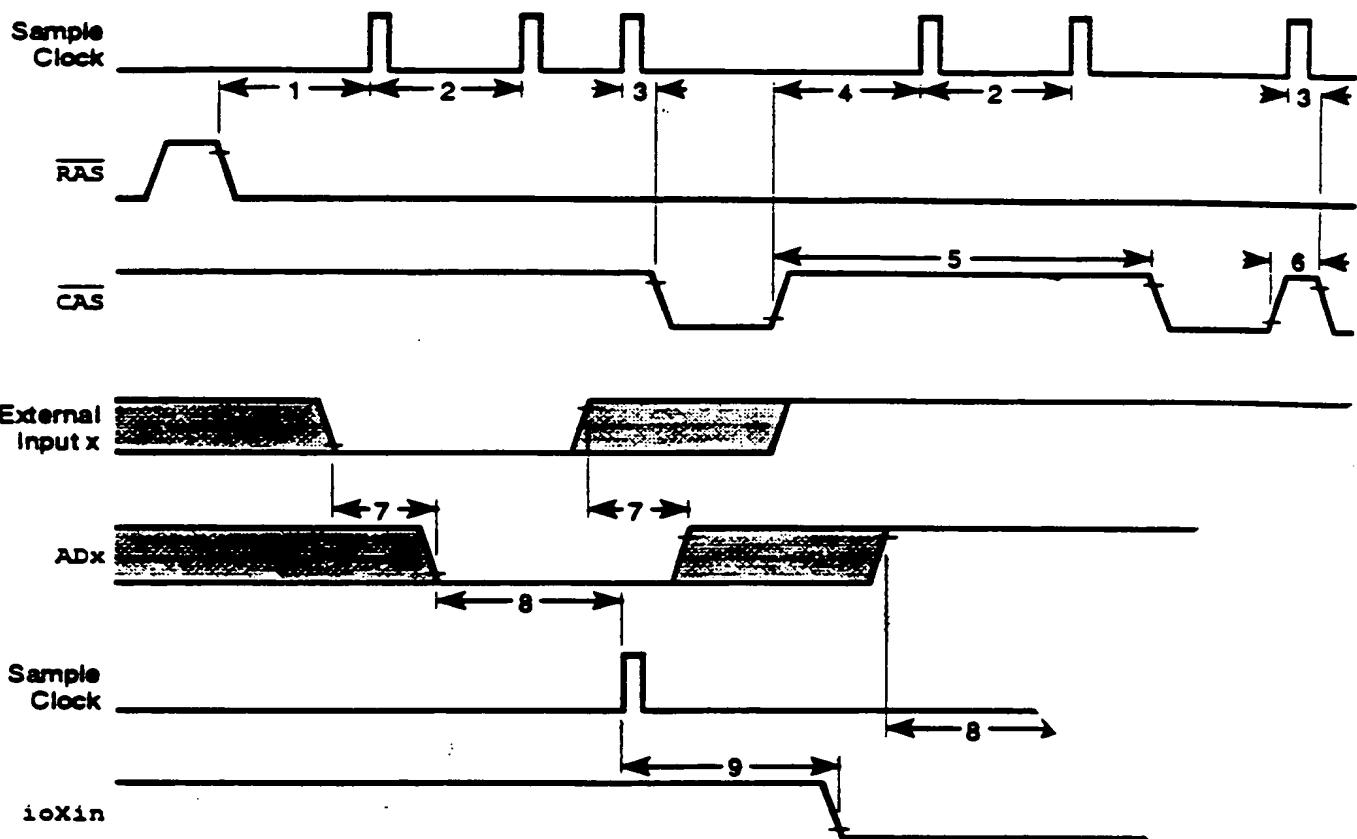


FIG. 76

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

BLACK BORDERS

IMAGE CUT OFF AT TOP, BOTTOM OR SIDES

FADED TEXT OR DRAWING

BLURRED OR ILLEGIBLE TEXT OR DRAWING

SKEWED/SLANTED IMAGES

COLOR OR BLACK AND WHITE PHOTOGRAPHS

GRAY SCALE DOCUMENTS

LINES OR MARKS ON ORIGINAL DOCUMENT

REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY

OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.